



H61H2-A

Rev : 1.0

ECS CONFIDENTIAL

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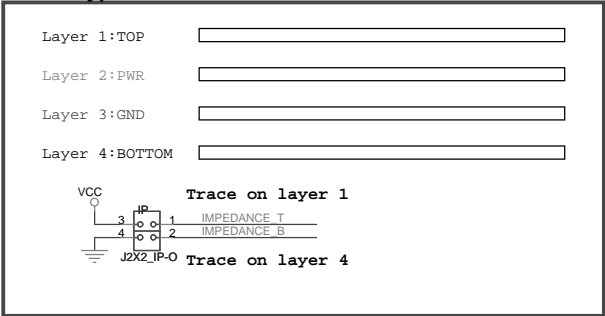
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REVISION HISTORY:

| Rev | Date | Notes |
|-------|-----------------------------|---|
| V.A | 2010/12/16 | Change from H67H2-M3: 1. Rear IO(VGA and DVI) 2. Three PCIEX1 Slots 3. Super IO change to IT8728 4. CPU PWM and VCCIO change to UPI 5. Remove USB3.0 6. Remove EZ Charger |
| V.1.0 | 2011/01/20 81-605-Y96100 | Change from V.A: 1.All-Solid Capacitor 2.Fix EZ charger 3. RT to 0402 |

Component
893PCS

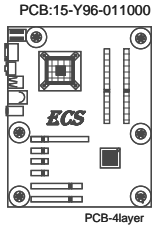
Circuit type 1



PCB Impedance control

| Impedance (OHM) | Trace Width (mil) (S/W/S) | Trace Length (inch) | Pre-preg | Default |
|-----------------|---------------------------|---------------------|----------|------------|
| 50 | 4 (16/4/16) | 8 | 1080 | TOP BOTTOM |
| 60 | 5 (20/5/20) | 10 | 2116 | INT |

PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM



PCB-4layer

RD - ELI
LAYOUT : Bing

NOTE:

Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev1_5.pdf
443554_443554_Intel6Series_C200Series_Chipset_EDS_Rev1_5.pdf

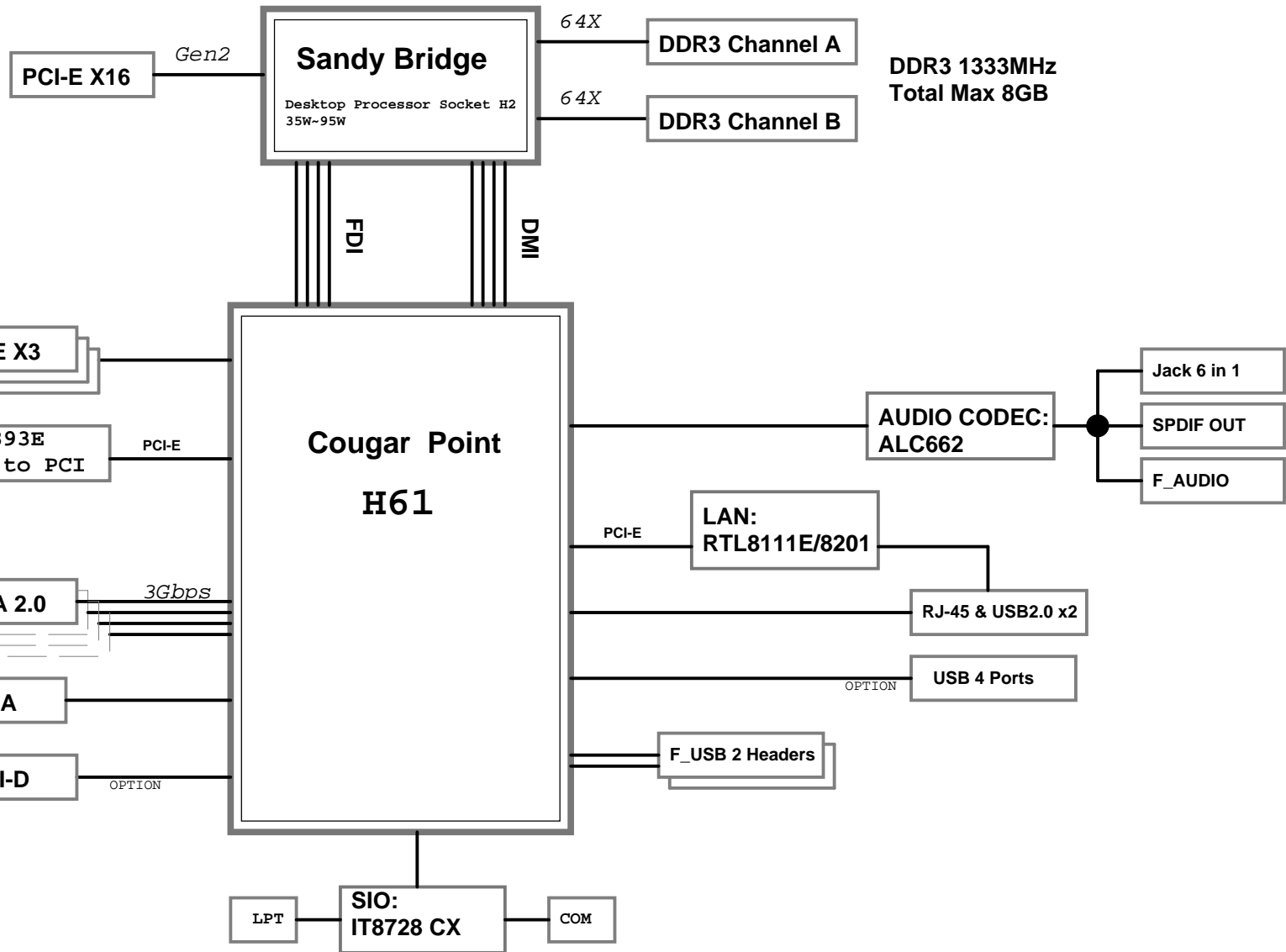


Elitegroup Computer Systems

| | | | |
|--------|----------------------------|------------|---------|
| Title | | Cover Page | |
| Size | Document Number | H61H2-A | |
| Custom | | Rev | 1.0 |
| Date: | Thursday, January 27, 2011 | Sheet | 1 of 31 |

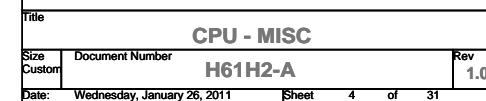
PCH-GPIO function

| Pin Name | Power Well | Usage | Default Status |
|----------|------------|-------------------|----------------|
| GPIO71 | VCC3 | | GPI |
| GPIO22 | VCC3 | | GPI |
| GPIO38 | VCC3 | | GPI |
| GPIO39 | VCC3 | | GPI |
| GPIO48 | VCC3 | | GPI |
| GPIO21 | VCC3 | | GPI |
| GPIO36 | VCC3 | | GPI |
| GPIO37 | VCC3 | | GPI |
| GPIO16 | VCC3 | Reserve for TPM | GPI |
| GPIO49 | VCC3 | Reserve for TPM | GPI |
| GPIO0 | VCC3 | F_AUDIO Detect | GPI |
| GPIO33 | VCC3 | ME Enable/Disable | GPO |
| GPIO34 | VCC3 | pull-up | GPI |
| GPIO13 | 3VSB | PME | GPI |
| GPIO24 | 3VSB | SKTOCC | GPO |
| GPIO57 | 3VSB | Board ID(CRB_0.7) | GPI |
| GPIO61 | 3VSB | TPM_LPCPD | GPI |



SIO-GPIO function

| Pin Name | Power Well | Usage | Default Status |
|----------|------------|-----------|----------------|
| GP16 | VCC3 | BEEP | |
| GP23 | | Power LED | |
| GP22 | | Power LED | |
| Pin Name | | Usage | |
| Pin Name | | Usage | |
| Pin Name | | Usage | |
| Pin Name | | Usage | |



| | |
|-------------------|--------------------|
| 7 M_DATA_A[0..63] | »» M_DATA A[0..63] |
| 7 M_DQS_A_P[0..7] | »» M DQS A P[0..7] |
| 7 M_DQS_A_N[0..7] | »» M DQS A N[0..7] |
| 7 M_MA_A[0..15] | »» M MA A[0..15] |
| 7 M_BS_A[0..2] | »» M BS A[0..2] |
| 7 M_CS_A_L[0..1] | »» M CS A L[0..1] |
| 7 M_CKE_A[0..1] | »» M CKE A[0..1] |
| 7 M_ODT_A[0..1] | »» M ODT A[0..1] |
| 7 M_CLK_A_P[0..1] | »» M CLK A P[0..1] |
| 7 M_CLK_A_N[0..1] | »» M CLK A N[0..1] |
| 7 M_WE_A_L | »» M WE A L |
| 7 M_CAS_A_L | »» M CAS A L |
| 7 M_RAS_A_L | »» M RAS A L |

DDR3 CH.A

7,8 DDR3_DRAMRST_L »» DDR3_DRAMRST_L

| | |
|-------------------|--------------------|
| 8 M_DATA_B[0..63] | »» M_DATA B[0..63] |
| 8 M_DQS_B_P[0..7] | »» M DQS B P[0..7] |
| 8 M_DQS_B_N[0..7] | »» M DQS B N[0..7] |
| 8 M_MA_B[0..15] | »» M MA B[0..15] |
| 8 M_BS_B[0..2] | »» M BS B[0..2] |
| 8 M_CS_B_L[0..1] | »» M CS B L[0..1] |
| 8 M_CKE_B[0..1] | »» M CKE B[0..1] |
| 8 M_ODT_B[0..1] | »» M ODT B[0..1] |
| 8 M_CLK_B_P[0..1] | »» M CLK B P[0..1] |
| 8 M_CLK_B_N[0..1] | »» M CLK B N[0..1] |
| 8 M_WE_B_L | »» M WE B L |
| 8 M_CAS_B_L | »» M CAS B L |
| 8 M_RAS_B_L | »» M RAS B L |

DDR3 CH.B

| CPUC | | | BALLMAP_REV=1.4 | | |
|------------|------|-----------|-----------------|------|----------------|
| M_DATA_A0 | AJ3 | SA_DQ_0 | SA_MA_0 | AV27 | M_MA_A0 |
| M_DATA_A1 | AJ4 | SA_DQ_1 | SA_MA_1 | AV24 | M_MA_A1 |
| M_DATA_A2 | AL3 | SA_DQ_2 | SA_MA_2 | AW24 | M_MA_A2 |
| M_DATA_A3 | AL4 | SA_DQ_3 | SA_MA_3 | AV23 | M_MA_A3 |
| M_DATA_A4 | AJ2 | SA_DQ_4 | SA_MA_4 | AV23 | M_MA_A4 |
| M_DATA_A5 | AJ1 | SA_DQ_5 | SA_MA_5 | AT24 | M_MA_A5 |
| M_DATA_A6 | AL2 | SA_DQ_6 | SA_MA_6 | AT23 | M_MA_A6 |
| M_DATA_A7 | AL1 | SA_DQ_7 | SA_MA_7 | AJ22 | M_MA_A7 |
| M_DATA_A8 | AN1 | SA_DQ_8 | SA_MA_8 | AV22 | M_MA_A8 |
| M_DATA_A9 | AR3 | SA_DQ_9 | SA_MA_9 | AT22 | M_MA_A9 |
| M_DATA_A10 | AR4 | SA_DQ_10 | SA_MA_10 | AV28 | M_MA_A10 |
| M_DATA_A11 | AN2 | SA_DQ_11 | SA_MA_11 | AJ21 | M_MA_A11 |
| M_DATA_A12 | AN3 | SA_DQ_12 | SA_MA_12 | AT21 | M_MA_A12 |
| M_DATA_A13 | AR2 | SA_DQ_13 | SA_MA_13 | AW32 | M_MA_A13 |
| M_DATA_A14 | AR1 | SA_DQ_14 | SA_MA_14 | AJ20 | M_MA_A14 |
| M_DATA_A15 | AV2 | SA_DQ_15 | SA_MA_15 | AT20 | M_MA_A15 |
| M_DATA_A16 | AW3 | SA_DQ_16 | | | |
| M_DATA_A17 | AV5 | SA_DQ_17 | | | |
| M_DATA_A18 | AW5 | SA_DQ_18 | SA_WE# | AW29 | M_WE_A_L |
| M_DATA_A19 | AJ2 | SA_DQ_19 | SA_CAS# | AV30 | M_CAS_A_L |
| M_DATA_A20 | AJ3 | SA_DQ_20 | SA_RAS# | AJ28 | M_RAS_A_L |
| M_DATA_A21 | AJ5 | SA_DQ_21 | | | |
| M_DATA_A22 | AJ5 | SA_DQ_22 | | | |
| M_DATA_A23 | AJ5 | SA_DQ_23 | SA_BS_0 | AY29 | M_BS_A0 |
| M_DATA_A24 | AY7 | SA_DQ_24 | SA_BS_1 | AW28 | M_BS_A1 |
| M_DATA_A25 | AJ7 | SA_DQ_25 | SA_BS_2 | AV20 | M_BS_A2 |
| M_DATA_A26 | AV9 | SA_DQ_26 | | | |
| M_DATA_A27 | AV7 | SA_DQ_27 | SA_CS#_0 | AJ29 | |
| M_DATA_A28 | AV7 | SA_DQ_28 | SA_CS#_1 | AV32 | |
| M_DATA_A29 | AW7 | SA_DQ_29 | SA_CS#_2 | AW30 | M_CS_A_L0 |
| M_DATA_A30 | AW9 | SA_DQ_30 | SA_CS#_3 | AJ33 | M_CS_A_L1 |
| M_DATA_A31 | AY3 | SA_DQ_31 | | | |
| M_DATA_A32 | AW37 | SA_DQ_32 | SA_CKE_0 | AV19 | |
| M_DATA_A33 | AW39 | SA_DQ_33 | SA_CKE_1 | AT18 | |
| M_DATA_A34 | AJ36 | SA_DQ_34 | SA_CKE_2 | AJ18 | M_CKE_A0 |
| M_DATA_A35 | AW36 | SA_DQ_35 | SA_CKE_3 | AV18 | M_CKE_A1 |
| M_DATA_A36 | AW38 | SA_DQ_36 | | | |
| M_DATA_A37 | AJ38 | SA_DQ_37 | | | |
| M_DATA_A38 | AJ37 | SA_DQ_38 | | | |
| M_DATA_A39 | AR40 | SA_DQ_39 | | | |
| M_DATA_A40 | AR37 | SA_DQ_40 | | | |
| M_DATA_A41 | AN37 | SA_DQ_41 | | | |
| M_DATA_A42 | AR39 | SA_DQ_42 | SA_ODT_0 | AV31 | |
| M_DATA_A43 | AR38 | SA_DQ_43 | SA_ODT_1 | AJ32 | M_ODT_A0 |
| M_DATA_A44 | AN38 | SA_DQ_44 | SA_ODT_2 | AJ30 | M_ODT_A1 |
| M_DATA_A45 | AN39 | SA_DQ_45 | SA_ODT_3 | AW33 | |
| M_DATA_A46 | AN40 | SA_DQ_46 | | | |
| M_DATA_A47 | AL40 | SA_DQ_47 | | | |
| M_DATA_A48 | AL37 | SA_DQ_48 | | | |
| M_DATA_A49 | AL39 | SA_DQ_49 | SA_CK_0 | AY25 | |
| M_DATA_A50 | AL38 | SA_DQ_50 | SA_CK_1 | AW25 | |
| M_DATA_A51 | AL39 | SA_DQ_51 | SA_CK_2 | AJ24 | |
| M_DATA_A52 | AL38 | SA_DQ_52 | SA_CK_3 | AW25 | |
| M_DATA_A53 | AJ39 | SA_DQ_53 | SA_CK_4 | AW27 | M_CLK_A_P0 |
| M_DATA_A54 | AJ40 | SA_DQ_54 | SA_CK_5 | AY27 | M_CLK_A_N0 |
| M_DATA_A55 | AG40 | SA_DQ_55 | SA_CK_6 | AW26 | M_CLK_A_P1 |
| M_DATA_A56 | AG37 | SA_DQ_56 | SA_CK_7 | AW26 | M_CLK_A_N1 |
| M_DATA_A57 | AE38 | SA_DQ_57 | | | |
| M_DATA_A58 | AE37 | SA_DQ_58 | | | |
| M_DATA_A59 | AE37 | SA_DQ_59 | | | |
| M_DATA_A60 | AG38 | SA_DQ_60 | SM_DRAMRST# | AW18 | DDR3_DRAMRST_L |
| M_DATA_A61 | AE39 | SA_DQ_61 | | | |
| M_DATA_A62 | AE40 | SA_DQ_62 | | | |
| M_DATA_A63 | AE40 | SA_DQ_63 | | | |
| M_DQS_A_P0 | AK3 | SA_DQS_0 | SA_DQS_8 | AV13 | |
| M_DQS_A_P1 | AP3 | SA_DQS_1 | SA_DQS#_8 | AV14 | |
| M_DQS_A_P2 | AW4 | SA_DQS_2 | | | |
| M_DQS_A_P3 | AV8 | SA_DQS_3 | | | |
| M_DQS_A_P4 | AJ37 | SA_DQS_4 | SA_ECC_CB_0 | AJ12 | |
| M_DQS_A_P5 | AP38 | SA_DQS_5 | SA_ECC_CB_1 | AJ14 | |
| M_DQS_A_P6 | AK38 | SA_DQS_6 | SA_ECC_CB_2 | AW13 | |
| M_DQS_A_P7 | AF38 | SA_DQS_7 | SA_ECC_CB_3 | AJ13 | |
| | | | SA_ECC_CB_4 | AJ13 | |
| | | | SA_ECC_CB_5 | AJ11 | |
| | | | SA_ECC_CB_6 | AW12 | |
| | | | SA_ECC_CB_7 | AW12 | |
| M_DQS_A_N0 | AK2 | SA_DQS#_0 | | | |
| M_DQS_A_N1 | AP2 | SA_DQS#_1 | | | |
| M_DQS_A_N2 | AV4 | SA_DQS#_2 | | | |
| M_DQS_A_N3 | AW8 | SA_DQS#_3 | | | |
| M_DQS_A_N4 | AV36 | SA_DQS#_4 | | | |
| M_DQS_A_N5 | AP39 | SA_DQS#_5 | | | |
| M_DQS_A_N6 | AK39 | SA_DQS#_6 | | | |
| M_DQS_A_N7 | AF39 | SA_DQS#_7 | | | |

SKT_H2_CRB

DDR3 CH.A

DDR_0

3 OF 10

Pay Attention to
This Part!


| CPUD | | | BALLMAP_REV=1.4 | | |
|------------|------|-----------|-----------------|------|------------|
| M_DATA_B0 | AG7 | SB_DQ_0 | SB_MA_0 | AK24 | M_MA_B0 |
| M_DATA_B1 | AG8 | SB_DQ_1 | SB_MA_1 | AM20 | M_MA_B1 |
| M_DATA_B2 | AJ9 | SB_DQ_2 | SB_MA_2 | AM19 | M_MA_B2 |
| M_DATA_B3 | AG6 | SB_DQ_3 | SB_MA_3 | AK18 | M_MA_B3 |
| M_DATA_B4 | AG5 | SB_DQ_4 | SB_MA_4 | AP19 | M_MA_B4 |
| M_DATA_B5 | AJ6 | SB_DQ_5 | SB_MA_5 | AP18 | M_MA_B5 |
| M_DATA_B6 | AJ7 | SB_DQ_6 | SB_MA_6 | AM18 | M_MA_B6 |
| M_DATA_B7 | AL7 | SB_DQ_7 | SB_MA_7 | AL18 | M_MA_B7 |
| M_DATA_B8 | AM7 | SB_DQ_8 | SB_MA_8 | AN18 | M_MA_B8 |
| M_DATA_B9 | AM10 | SB_DQ_9 | SB_MA_9 | AY17 | M_MA_B9 |
| M_DATA_B10 | AL10 | SB_DQ_10 | SB_MA_10 | AN23 | M_MA_B10 |
| M_DATA_B11 | AL6 | SB_DQ_11 | SB_MA_11 | AJ17 | M_MA_B11 |
| M_DATA_B12 | AM6 | SB_DQ_12 | SB_MA_12 | AU17 | M_MA_B12 |
| M_DATA_B13 | AL9 | SB_DQ_13 | SB_MA_13 | AT18 | M_MA_B13 |
| M_DATA_B14 | AM9 | SB_DQ_14 | SB_MA_14 | AR26 | M_MA_B14 |
| M_DATA_B15 | AP7 | SB_DQ_15 | SB_MA_15 | AY16 | M_MA_B15 |
| M_DATA_B16 | AR7 | SB_DQ_16 | | | |
| M_DATA_B17 | AP10 | SB_DQ_17 | | | |
| M_DATA_B18 | AR10 | SB_DQ_18 | SA_CK[2] | AR25 | M_WE_B_L |
| M_DATA_B19 | AP5 | SB_DQ_19 | SA_CK[1] | AK25 | M_CAS_B_L |
| M_DATA_B20 | AR6 | SB_DQ_20 | SA_ODT[2] | AP24 | M_RAS_B_L |
| M_DATA_B21 | AP9 | SB_DQ_21 | | | |
| M_DATA_B22 | AR9 | SB_DQ_22 | SB_BS_0 | AP23 | M_BS_B0 |
| M_DATA_B23 | AM12 | SB_DQ_23 | SB_BS_1 | AM24 | M_BS_B1 |
| M_DATA_B24 | AM13 | SB_DQ_24 | SB_BS_2 | AW17 | M_BS_B2 |
| M_DATA_B25 | AR13 | SB_DQ_25 | | | |
| M_DATA_B26 | AP13 | SB_DQ_26 | SB_CS#_0 | AN25 | |
| M_DATA_B27 | AL12 | SB_DQ_27 | SB_CS#_1 | AN26 | |
| M_DATA_B28 | AL13 | SB_DQ_28 | SB_CS#_2 | AL25 | M_CS_B_L0 |
| M_DATA_B29 | AR12 | SB_DQ_29 | SB_CS#_3 | AT26 | M_CS_B_L1 |
| M_DATA_B30 | AR12 | SB_DQ_30 | | | |
| M_DATA_B31 | AR28 | SB_DQ_31 | | | |
| M_DATA_B32 | AR29 | SB_DQ_32 | | | |
| M_DATA_B33 | AL28 | SB_DQ_33 | SB_CKE_0 | AU16 | |
| M_DATA_B34 | AL29 | SB_DQ_34 | SB_CKE_1 | AY15 | |
| M_DATA_B35 | AP28 | SB_DQ_35 | SB_CKE_2 | AW15 | M_CKE_B0 |
| M_DATA_B36 | AP29 | SB_DQ_36 | SB_CKE_3 | AV15 | M_CKE_B1 |
| M_DATA_B37 | AM28 | SB_DQ_37 | | | |
| M_DATA_B38 | AM29 | SB_DQ_38 | | | |
| M_DATA_B39 | AP32 | SB_DQ_39 | | | |
| M_DATA_B40 | AP31 | SB_DQ_40 | | | |
| M_DATA_B41 | AP34 | SB_DQ_41 | SB_ODT_0 | AL26 | |
| M_DATA_B42 | AP35 | SB_DQ_42 | SB_ODT_1 | AP26 | |
| M_DATA_B43 | AR32 | SB_DQ_43 | SB_ODT_2 | AM26 | M_ODT_B0 |
| M_DATA_B44 | AR31 | SB_DQ_44 | SB_ODT_3 | AK26 | M_ODT_B1 |
| M_DATA_B45 | AR35 | SB_DQ_45 | | | |
| M_DATA_B46 | AR35 | SB_DQ_46 | | | |
| M_DATA_B47 | AR34 | SB_DQ_47 | | | |
| M_DATA_B48 | AM31 | SB_DQ_48 | | | |
| M_DATA_B49 | AL35 | SB_DQ_49 | SB_CK_0 | AL21 | |
| M_DATA_B50 | AL32 | SB_DQ_50 | SB_CK_1 | AL22 | |
| M_DATA_B51 | AM34 | SB_DQ_51 | SB_CK_2 | AK20 | |
| M_DATA_B52 | AL31 | SB_DQ_52 | SB_CK_3 | AL23 | M_CLK_B_P0 |
| M_DATA_B53 | AM35 | SB_DQ_53 | | AM22 | M_CLK_B_N0 |
| M_DATA_B54 | AL34 | SB_DQ_54 | SB_CK_4 | AP21 | M_CLK_B_P1 |
| M_DATA_B55 | AH35 | SB_DQ_55 | SB_CK_5 | AN21 | M_CLK_B_N1 |
| M_DATA_B56 | AH34 | SB_DQ_56 | | | |
| M_DATA_B57 | AE34 | SB_DQ_57 | | | |
| M_DATA_B58 | AE35 | SB_DQ_58 | | | |
| M_DATA_B59 | AE35 | SB_DQ_59 | | | |
| M_DATA_B60 | AJ34 | SB_DQ_60 | | | |
| M_DATA_B61 | AF33 | SB_DQ_61 | | | |
| M_DATA_B62 | AF35 | SB_DQ_62 | | | |
| M_DATA_B63 | AF35 | SB_DQ_63 | | | |
| M_DQS_B_P0 | AH7 | SB_DQS_0 | SB_DQS_8 | AN16 | |
| M_DQS_B_P1 | AM8 | SB_DQS_1 | SB_DQS#_8 | AN15 | |
| M_DQS_B_P2 | AR8 | SB_DQS_2 | | | |
| M_DQS_B_P3 | AN13 | SB_DQS_3 | | | |
| M_DQS_B_P4 | AN29 | SB_DQS_4 | SB_ECC_CB_0 | AL18 | |
| M_DQS_B_P5 | AP33 | SB_DQS_5 | SB_ECC_CB_1 | AM16 | |
| M_DQS_B_P6 | AL33 | SB_DQS_6 | SB_ECC_CB_2 | AP16 | |
| M_DQS_B_P7 | AG35 | SB_DQS_7 | SB_ECC_CB_3 | AR16 | |
| | | | SB_ECC_CB_4 | AL15 | |
| | | | SB_ECC_CB_5 | AM15 | |
| | | | SB_ECC_CB_6 | AR15 | |
| | | | SB_ECC_CB_7 | AP15 | |
| M_DQS_B_N0 | AH6 | SB_DQS#_0 | | | |
| M_DQS_B_N1 | AL8 | SB_DQS#_1 | | | |
| M_DQS_B_N2 | AP8 | SB_DQS#_2 | | | |
| M_DQS_B_N3 | AN12 | SB_DQS#_3 | | | |
| M_DQS_B_N4 | AN28 | SB_DQS#_4 | | | |
| M_DQS_B_N5 | AR33 | SB_DQS#_5 | | | |
| M_DQS_B_N6 | AM33 | SB_DQS#_6 | | | |
| M_DQS_B_N7 | AG34 | SB_DQS#_7 | | | |

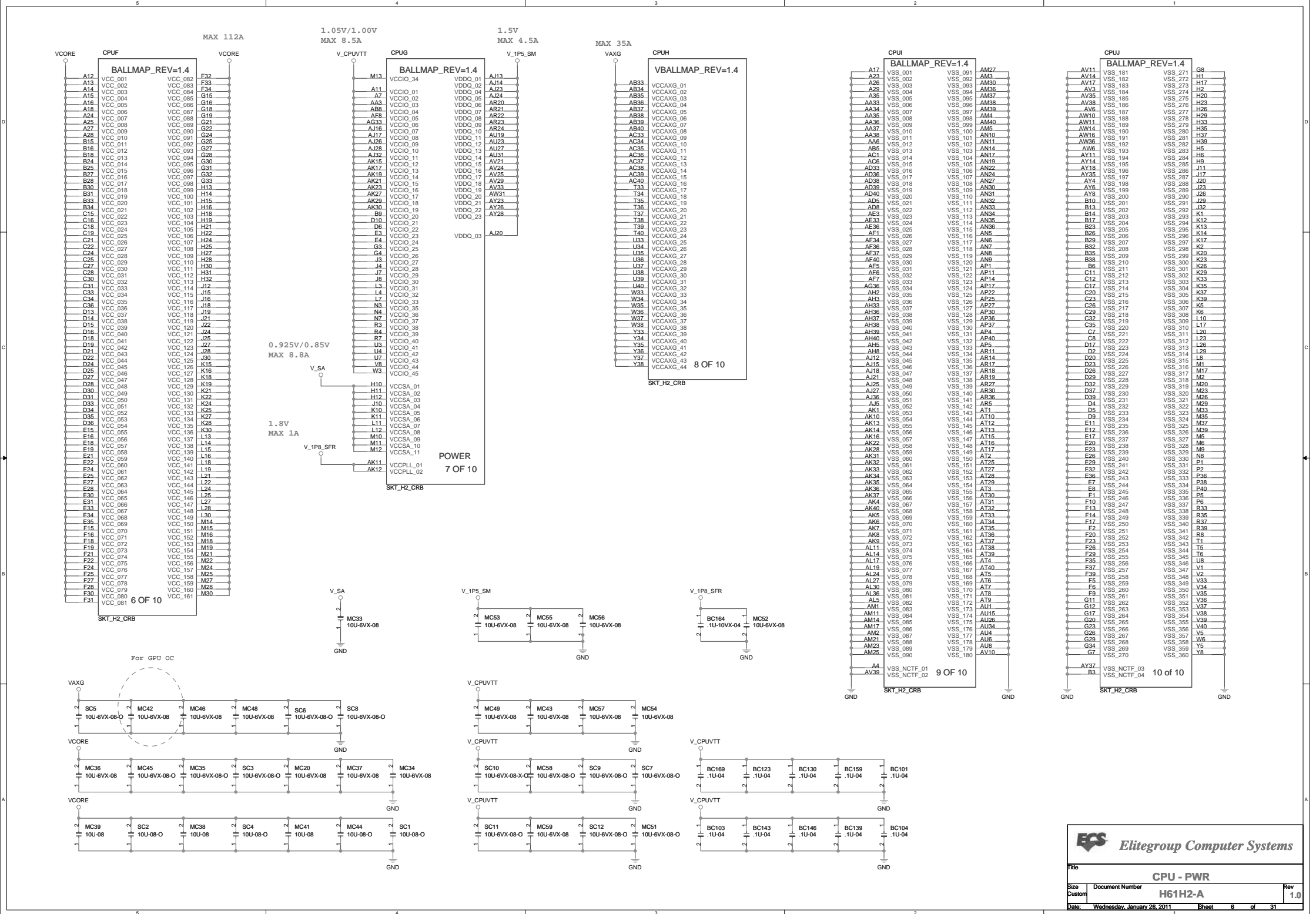
SKT_H2_CRB

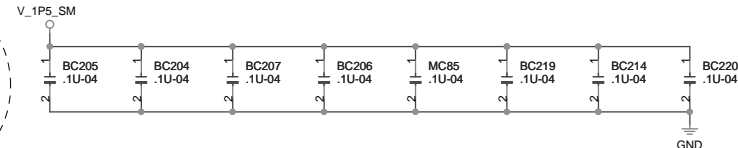
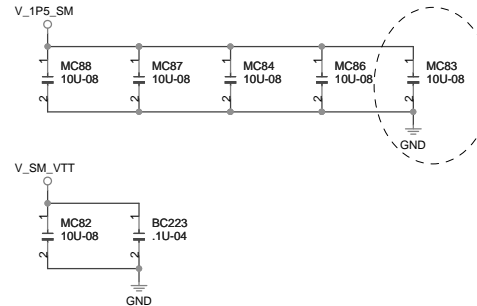
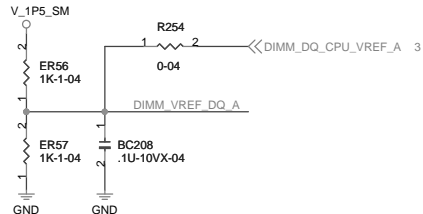
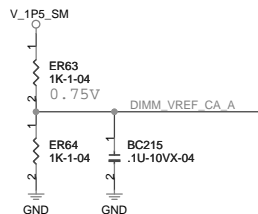
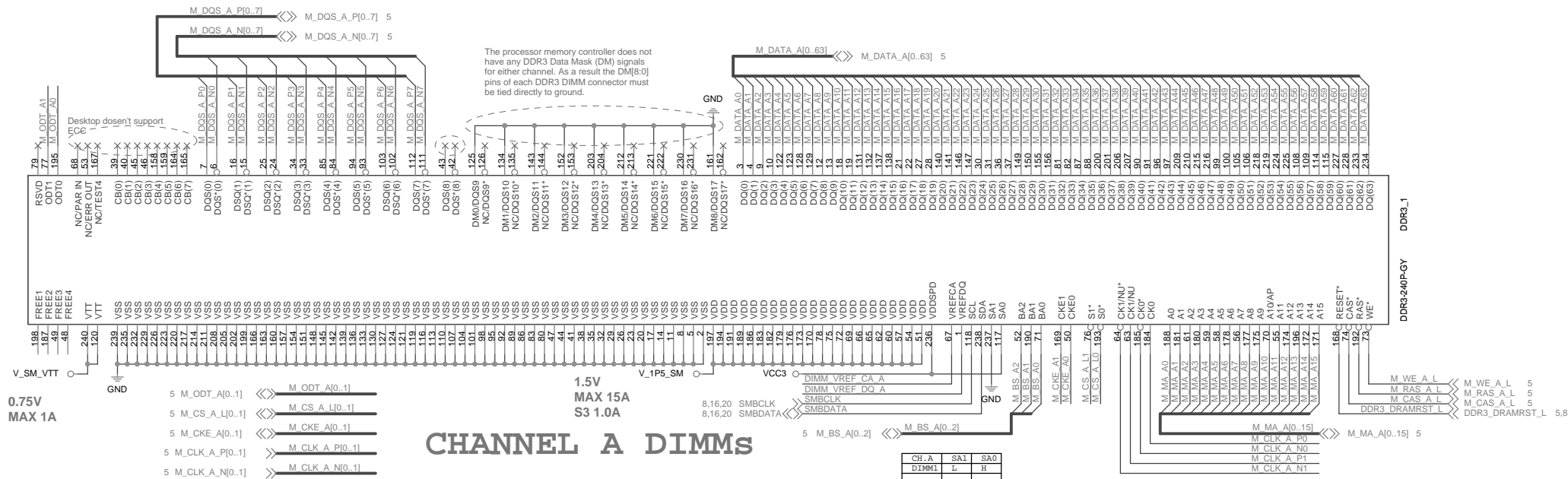
DDR3 CH.B

DDR_1

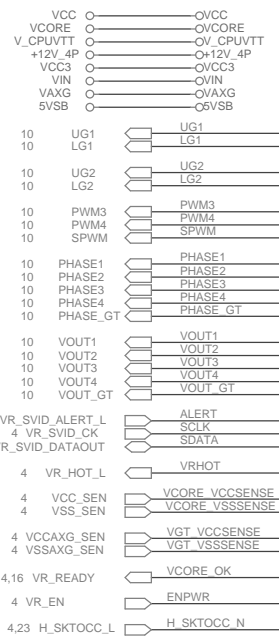
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| | | |
|--|-----------------------------|---------------|
|  Elitegroup Computer Systems | | |
| Title | | |
| CPU - DDR3 | | |
| Size | Document Number | Rev |
| Custon | H61H2-A | 1.0 |
| Date: | Wednesday, January 26, 2011 | Sheet 5 of 31 |



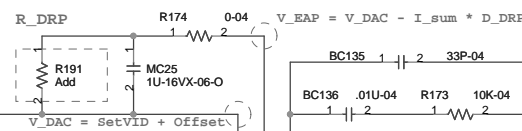


External Connection



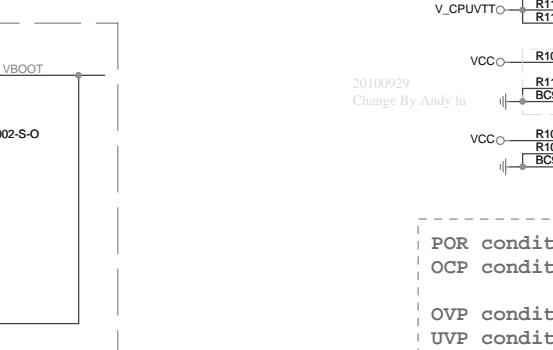
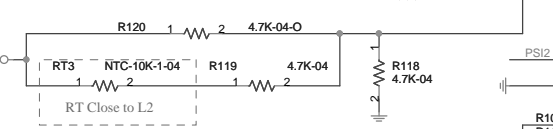
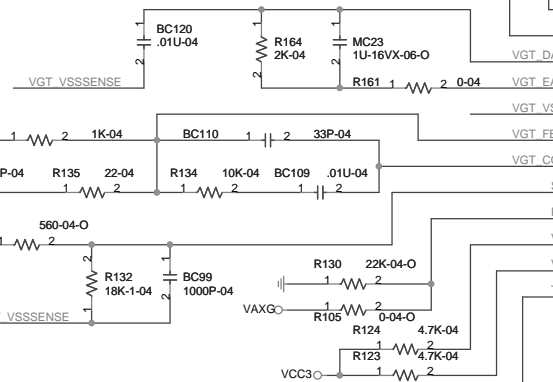
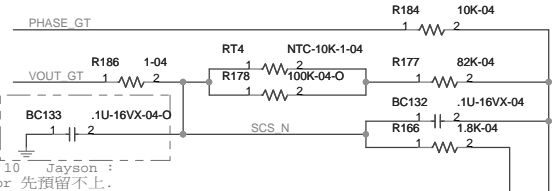
Css connect from DAC to FBRTN for SS and Dynamic VID.
 $T_{ss} = T_{dynamic} = V_{DAC} * C_{ss} / I_{ss}$, $V_{boot} = 0$
 $T_{ss} = (V_{DAC} - V_{boot}) * C_{ss} / I_{ss}$, $V_{boot} \neq 0$
 $I_{ss} = 200\mu A$, if SETVID = Fast (01H)
 $I_{ss} = 50\mu A$, if SETVID = Slow (02H)

Load Line = $DCR * R_{DRP} / (n * R_{csn})$

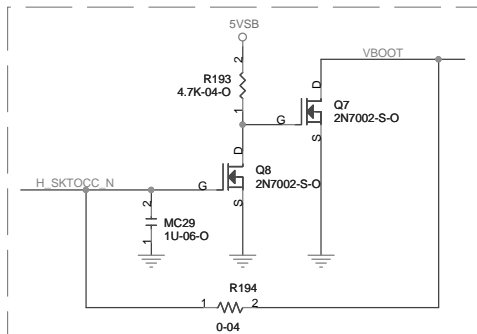


$V_{IMON} = I_{sum} * R_{IMON}$
 $I_{sum} = I_o * DCR / (n * R_{csn})$

Phase Frequency:
 $f_{sw} = 300 * (27k / RT) * 0.83$
 $RT = 25k \rightarrow f_{sw} = 300k \text{ Hz}$



1130'10 By Jayson add.
Page23, H_SKT0CC_N has
place pull high
resistor.



20100929
Change By Andy lu

POR condition: $V_{CC5} > 4.3V$ AND $V_{CC12} > 9.5V$ AND $ENPWR > 0.65V$
 OCP condition: $V_{IMON} > 1.3 * V_{IMAX}$ for total current
 $I_{CSNx} > 100\mu A$ for channel current
 OVP condition: $V_{FB} - V_{EAP} > 150mV$
 UVP condition: $V_{FB} < 200mV$

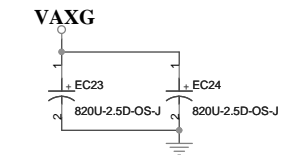
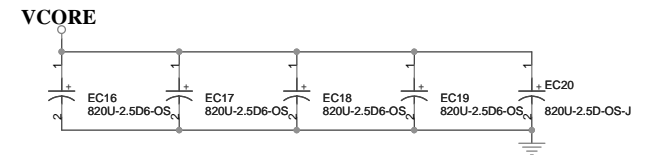
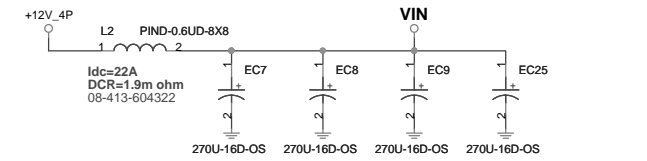
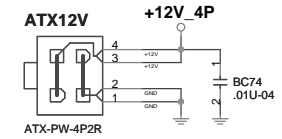
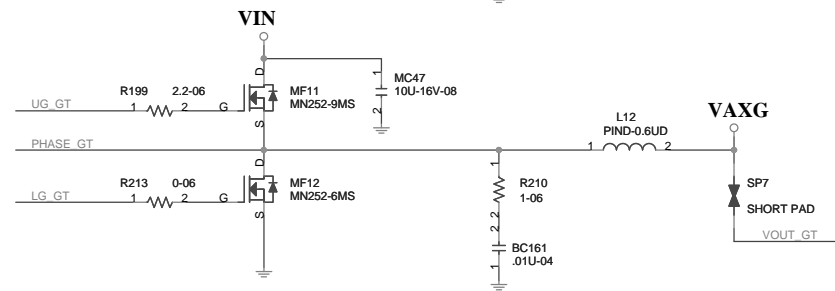
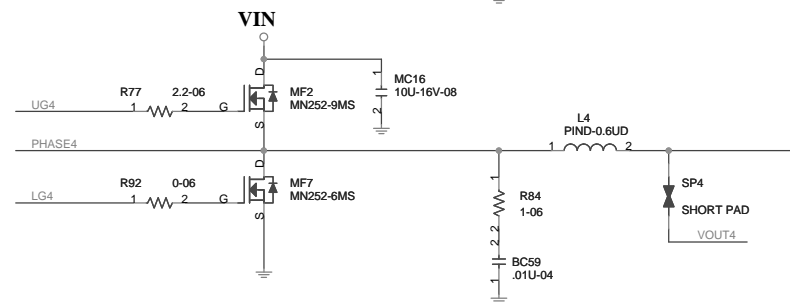
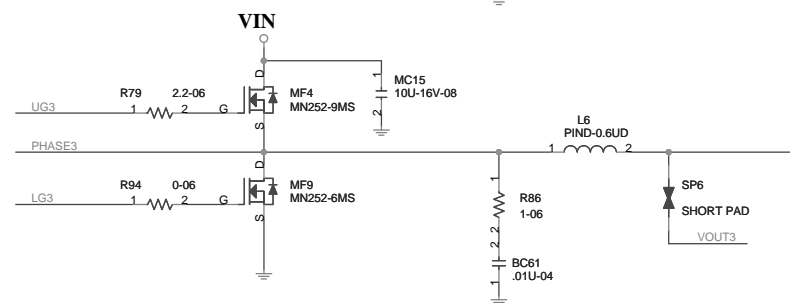
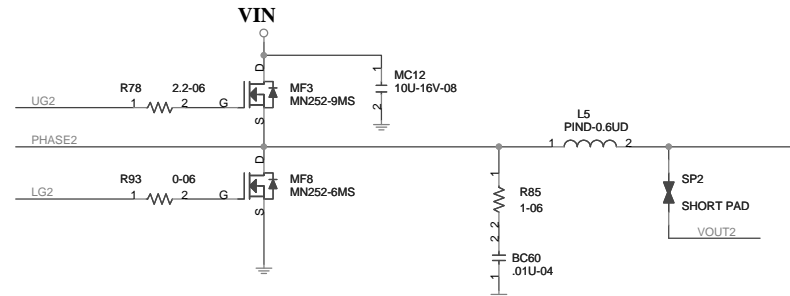
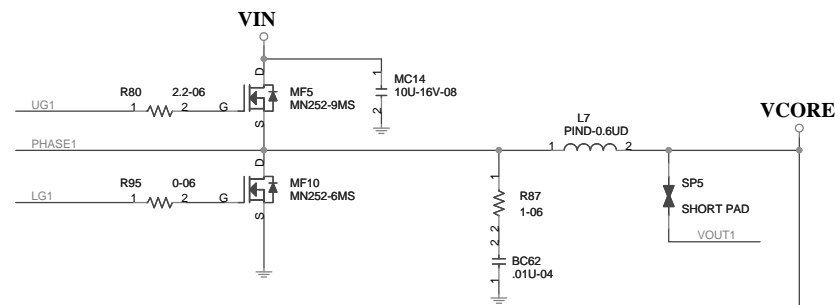
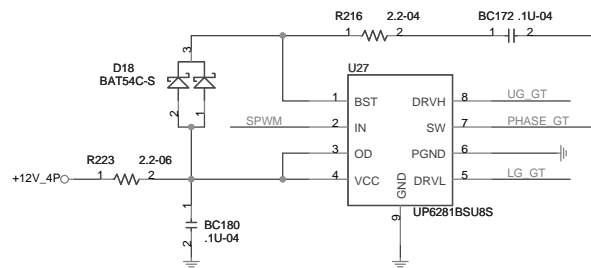
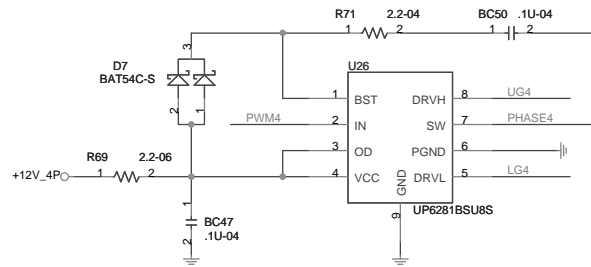
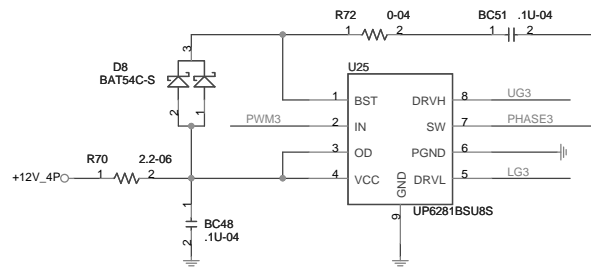
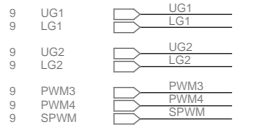
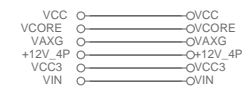
UP1625Q

VBOOT:
 VCC -> VCORE / VAXG boot 1.1V
 GND -> VCORE / VAXG boot 0V

Elitegroup Computer Systems

| | | | |
|--------|----------------------------|---------------------|---------|
| Title | | VCORE / VAXG UP1625 | |
| Size | Document Number | H61H2-A | |
| Custom | | Rev 1.0 | |
| Date: | Thursday, January 27, 2011 | Sheet | 9 of 31 |

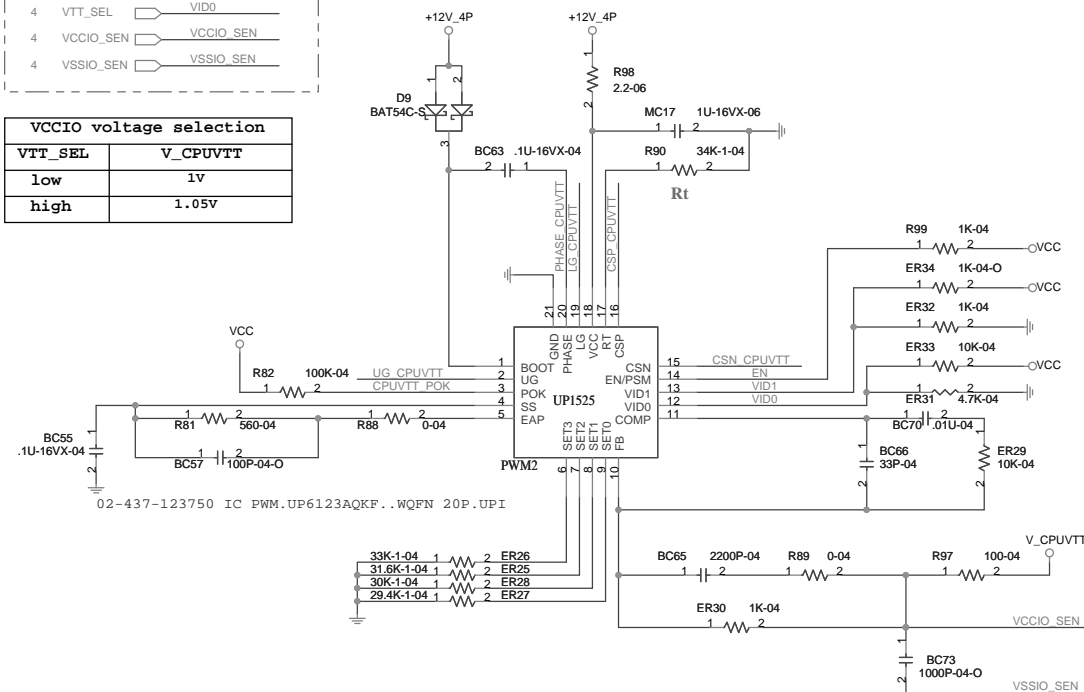
External Connection



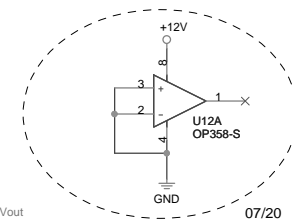
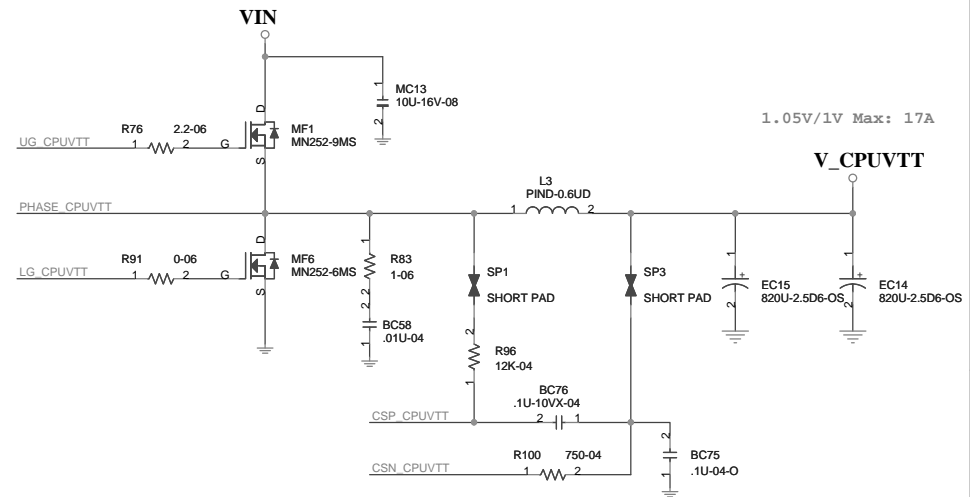
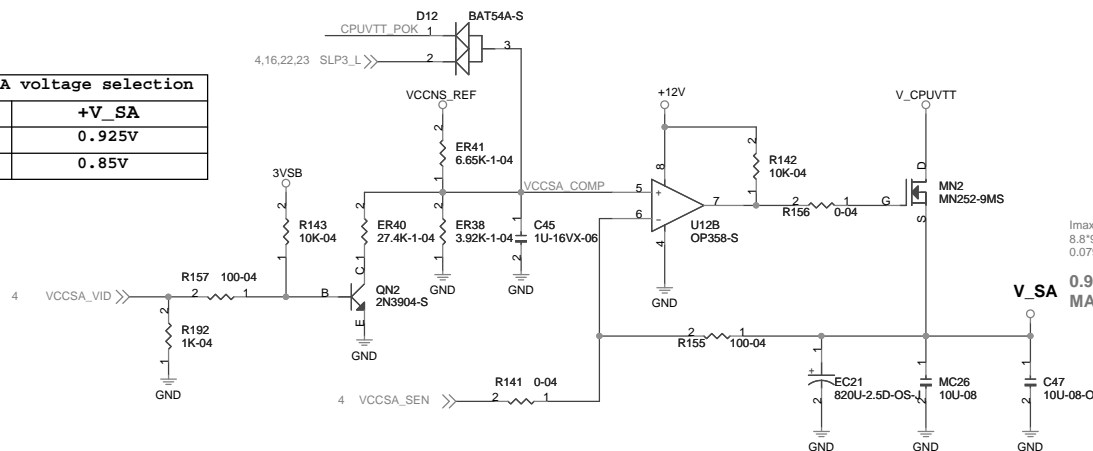
External Connection

| Pin | Signal | Signal |
|-------------|-------------|--------|
| VCC | OVCC | |
| 3VSB | OV_3VSB | |
| 5VSB | OV_CPUVTT | |
| V_1P05_PCH | OV_1P05_PCH | |
| V_CPUVTT | OV_CPUVTT | |
| 4 VTT_SEL | VTT_SEL | |
| 4 VCCIO_SEN | VCCIO_SEN | |
| 4 VSSIO_SEN | VSSIO_SEN | |

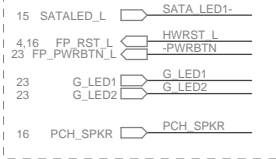
| VCCIO voltage selection | |
|-------------------------|----------|
| VTT_SEL | V_CPUVTT |
| low | 1v |
| high | 1.05V |



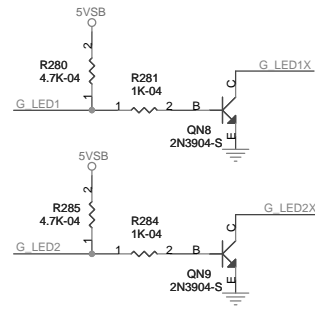
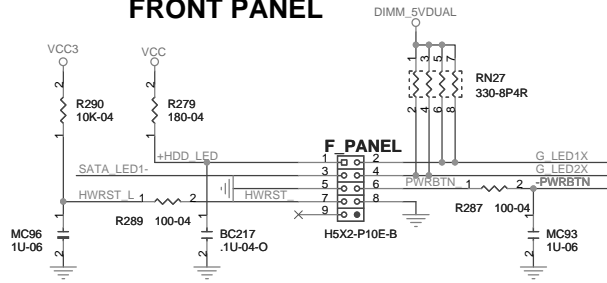
| VCCSA voltage selection | |
|-------------------------|--------|
| VID | +V_SA |
| 0 | 0.925V |
| 1 | 0.85V |



External Connection

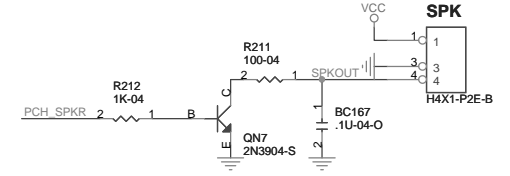


FRONT PANEL



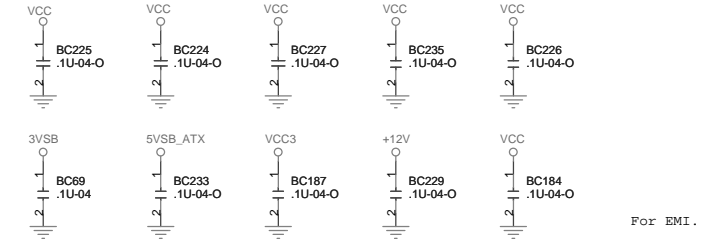
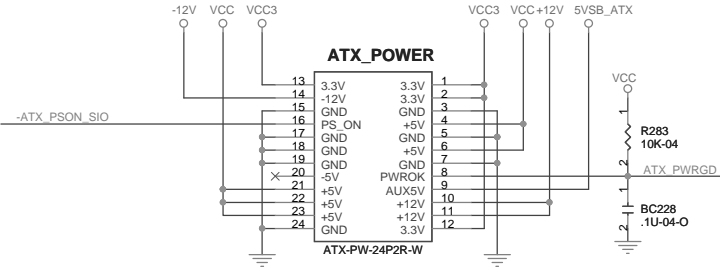
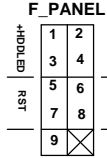
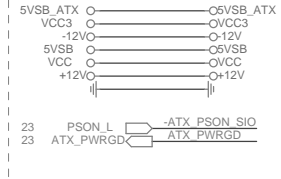
| | S0 | S1 | S3 | S4 | S5 |
|--------|----|----|-----|-----|-----|
| G_LED1 | L | B | B | L | L |
| G_LED2 | H | H | L | L | L |
| G | GB | YB | OFF | OFF | OFF |

B: Blinking



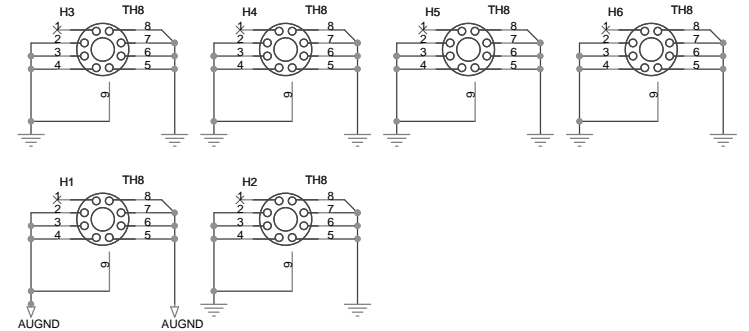
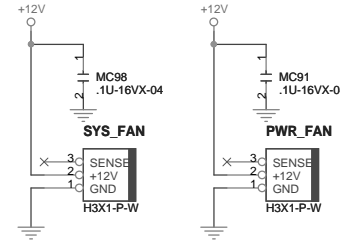
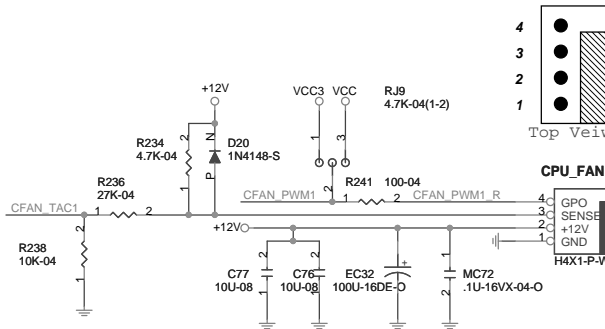
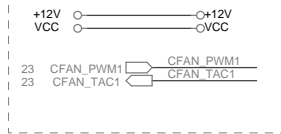
POWER CONNECTOR

External Connection



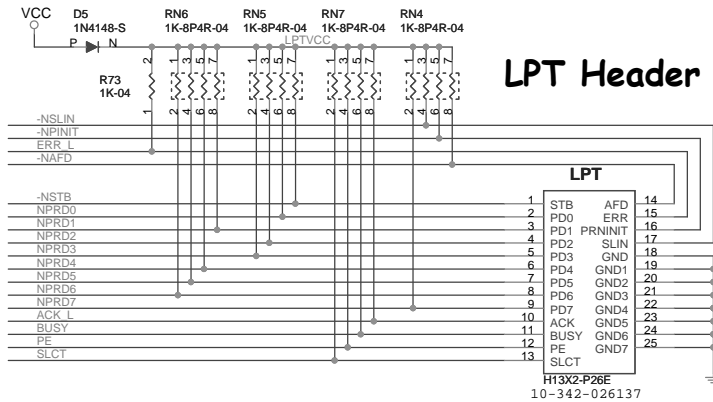
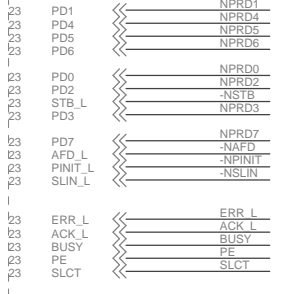
FAN

External Connection



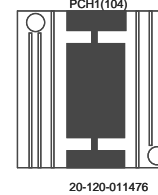
LPT Ports

External Connection

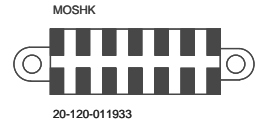


LPT Header

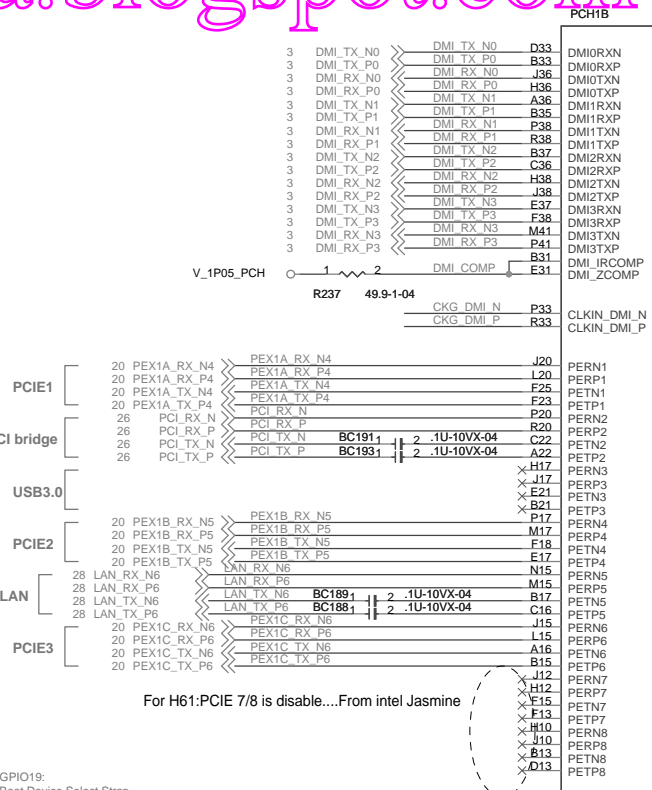
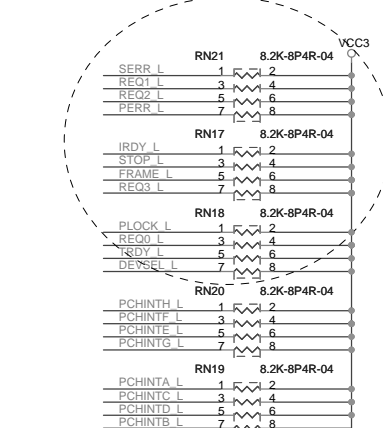
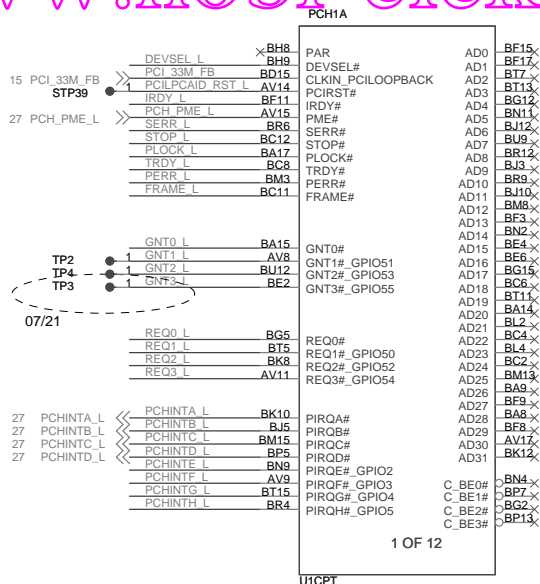
604



CLR_CMOS(1-2)



For H61:USB 6/7/12/13 is disable



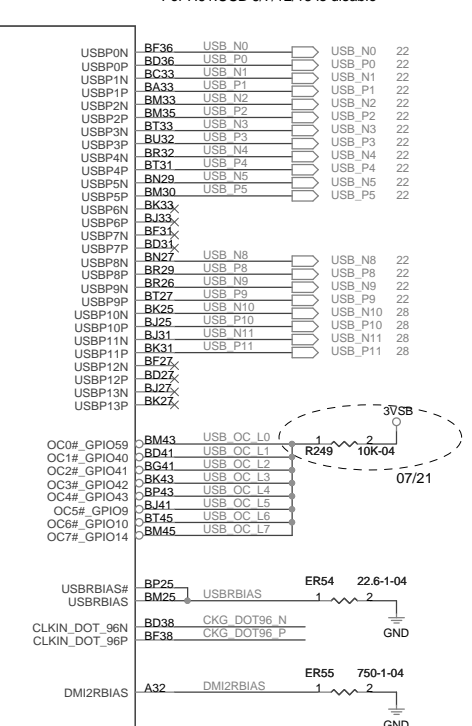
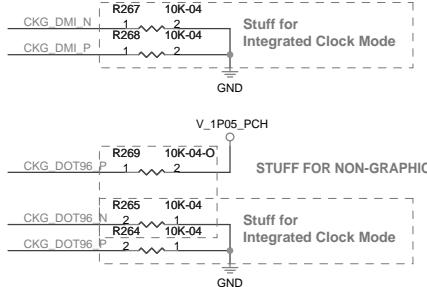
GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ESI Strap (Server Only),
DONT Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode,
When Sampled Low.

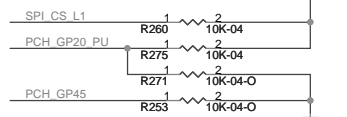
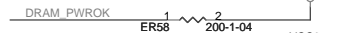
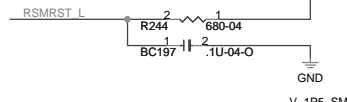
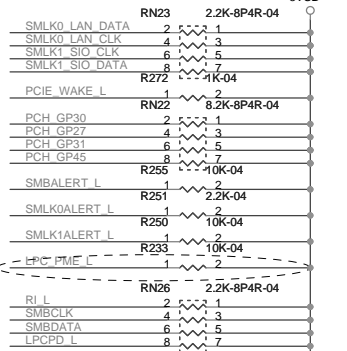
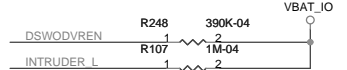
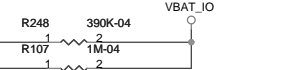
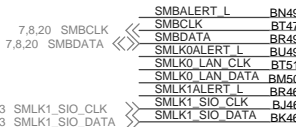
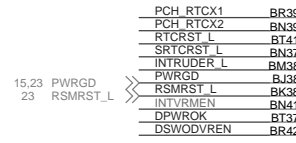
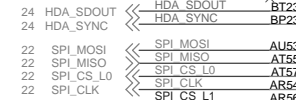
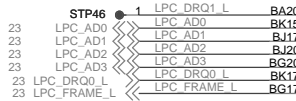


GNT[0..3]#
GPIO19
have been internal pull high to +VCC3

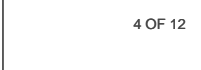
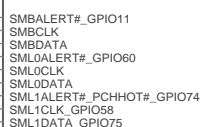
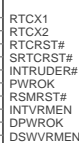
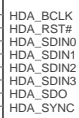
Boot Device Select:

| BOOT DEVICE | GNT1_L | GPIO19 |
|-------------|--------|--------|
| LPC | 0 | 0 |
| PCI | 1 | 0 |
| SPI | 1 | 1 |

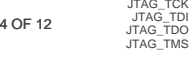
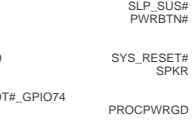
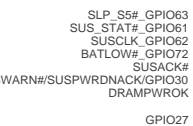
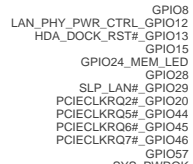
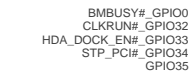
23 LPC_AD[0..3] L AD[0..3]



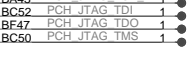
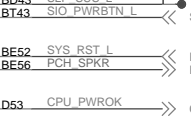
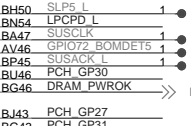
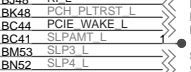
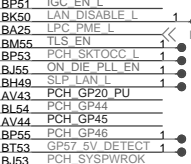
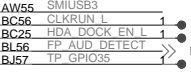
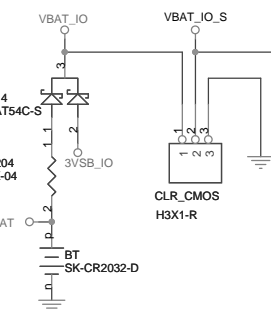
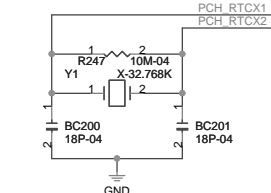
PCH1D



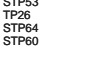
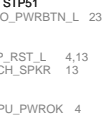
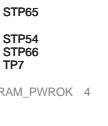
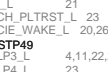
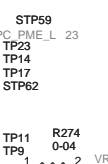
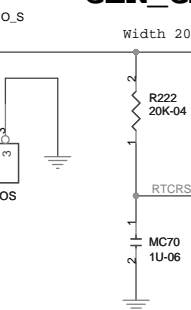
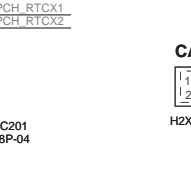
U1CPT



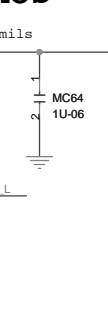
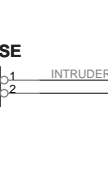
U1CPT



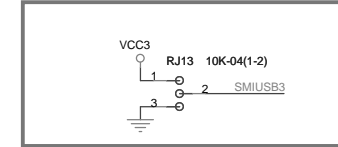
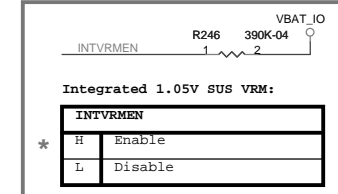
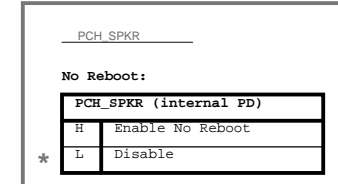
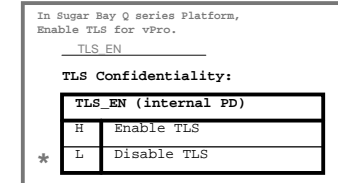
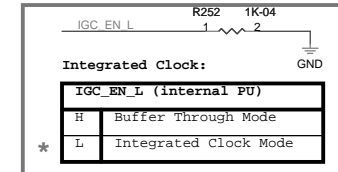
U1CPT



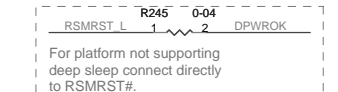
U1CPT



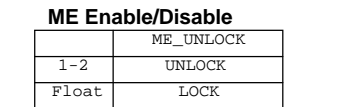
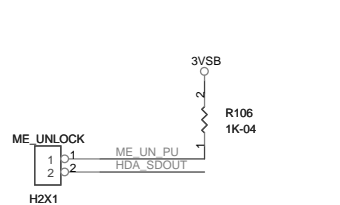
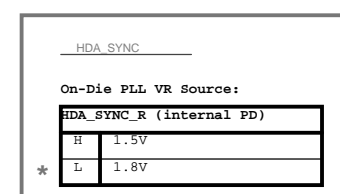
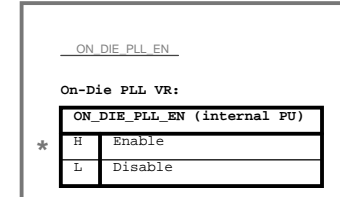
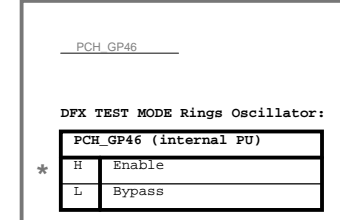
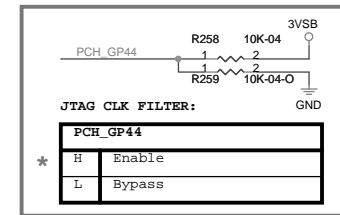
Buffer Through Mode / Integrated Clock Mode have been changed to F/W Strap. Default: Integrated Clock Mode. Doc. Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1

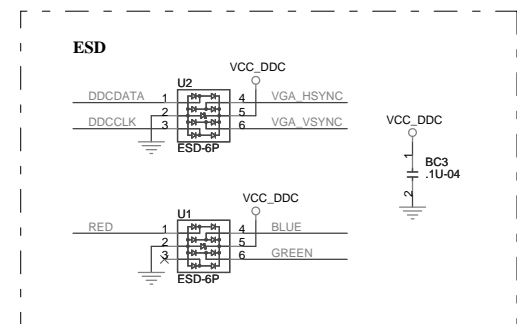
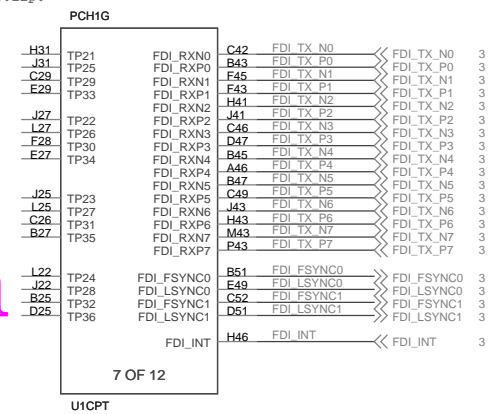
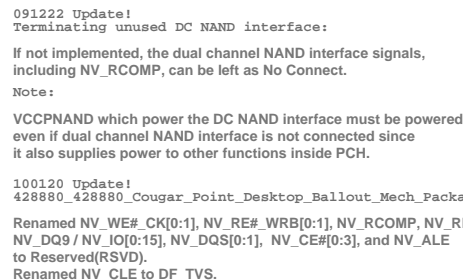


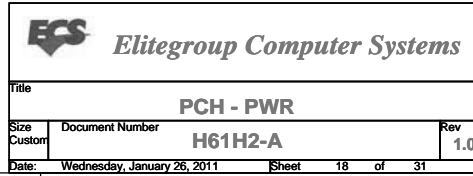
When Deep Sleep not implemented:
1.PCH_GP30, PCH_GP27 need to be Pull Up.
2.VCCDSW3_3 should to be connected to +3VSB.
3.SLP_SUS_L, SUSACK_L left unconnected.
4.SUSWARN_L may be used as GPIO30.(Reference to 1.)



For platform not supporting deep sleep connect directly to RSMRST#.





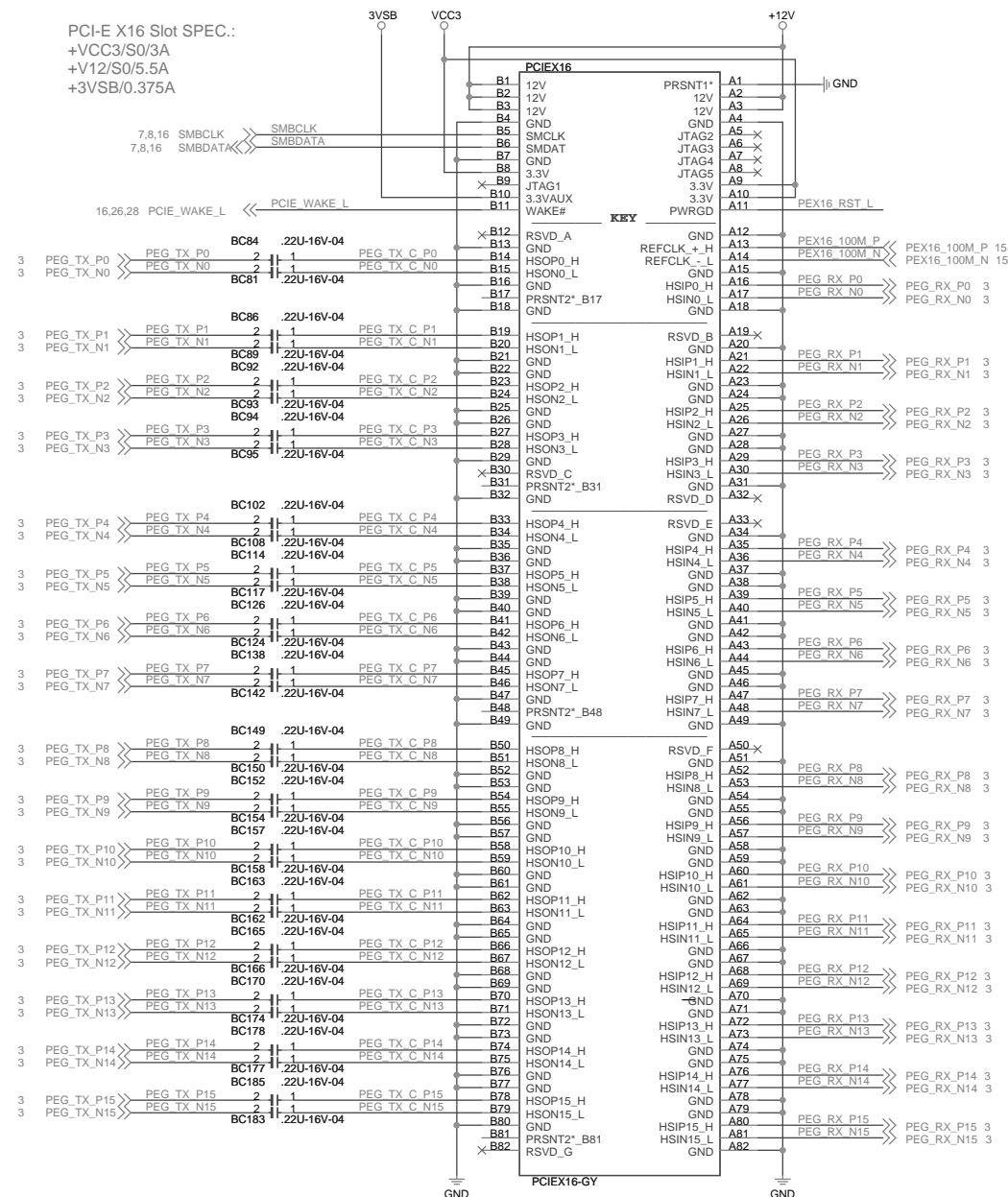


PCI-E X16 Slot SPEC.:

+VCC3/S0/3A

+V12/S0/5.5A

+3VSB/0.375A

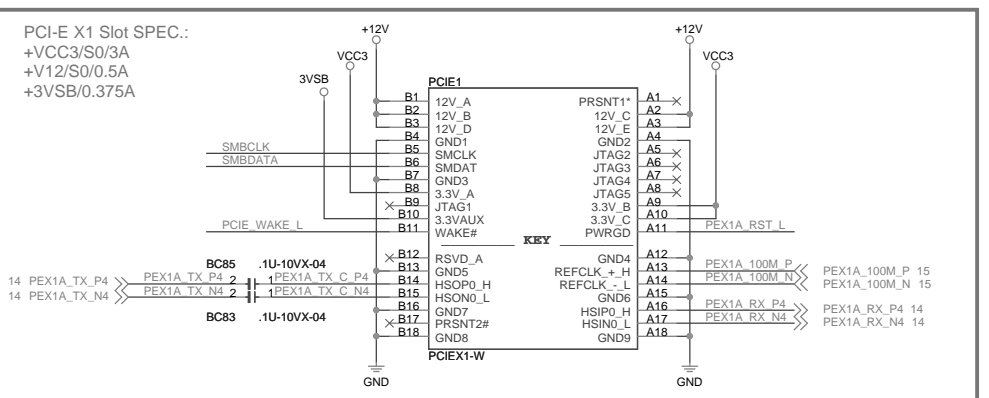


PCI-E X1 Slot SPEC.:

+VCC3/S0/3A

+V12/S0/0.5A

+3VSB/0.375A



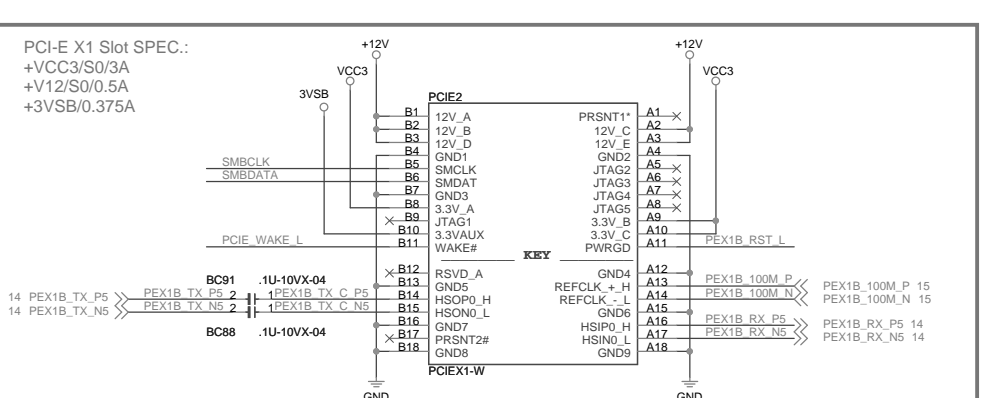
PCI-E X1 A

PCI-E X1 Slot SPEC.:

+VCC3/S0/3A

+V12/S0/0.5A

+3VSB/0.375A



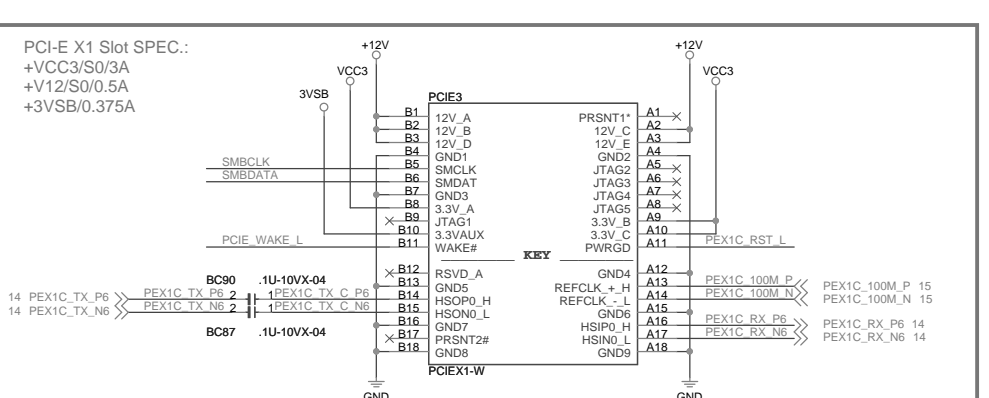
PCI-E X1 B

PCI-E X1 Slot SPEC.:

+VCC3/S0/3A

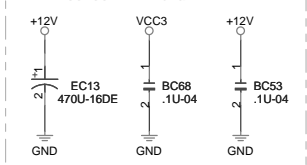
+V12/S0/0.5A

+3VSB/0.375A

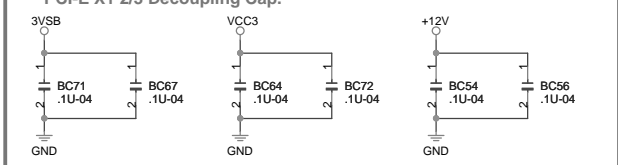


PCI-E X1 C

Between PEX16 & PEX1

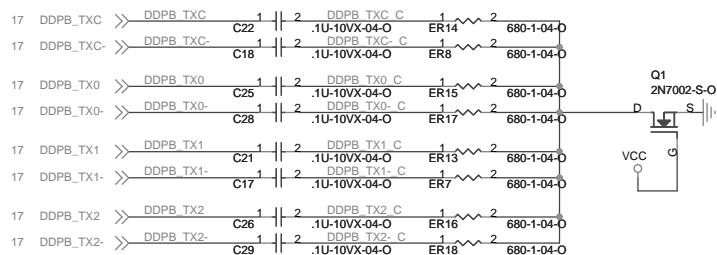


PCI-E X1 2/3 Decoupling Cap.

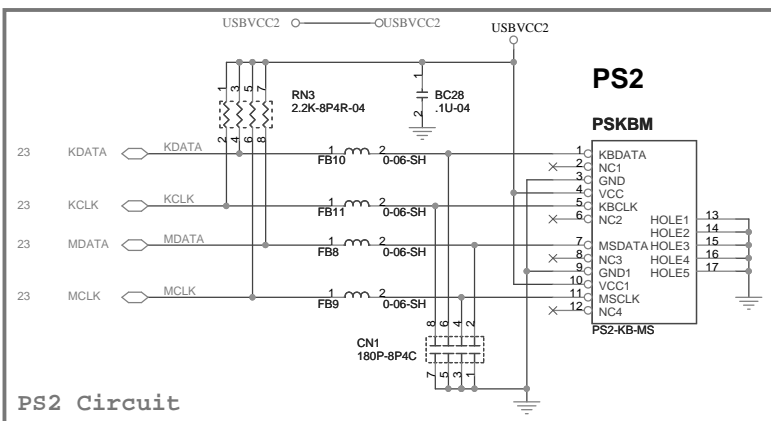
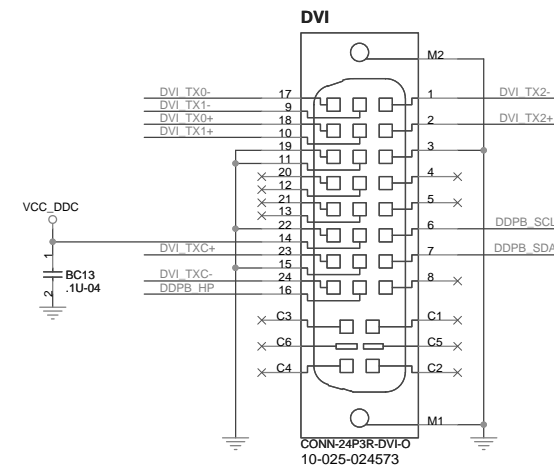
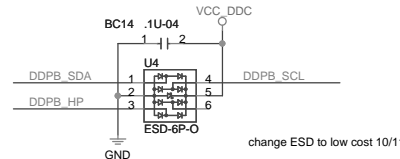
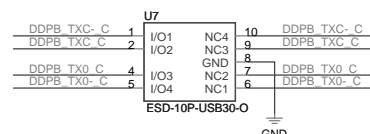
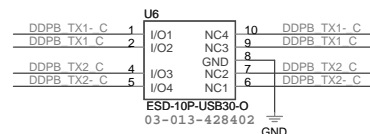
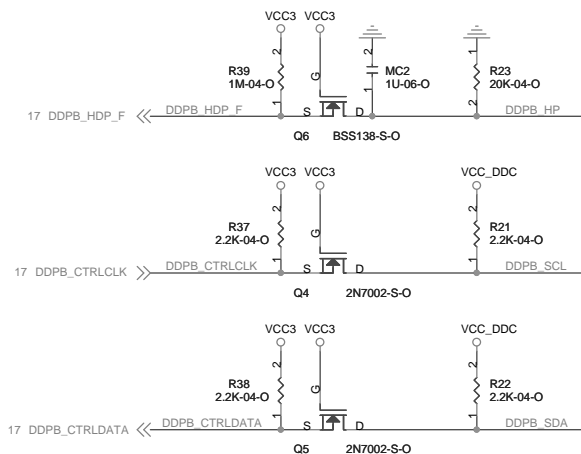
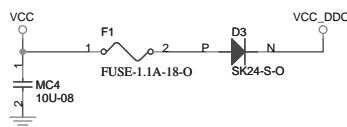
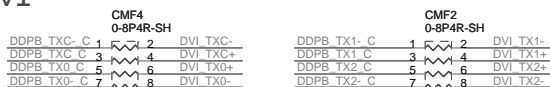


Elitegroup Computer Systems

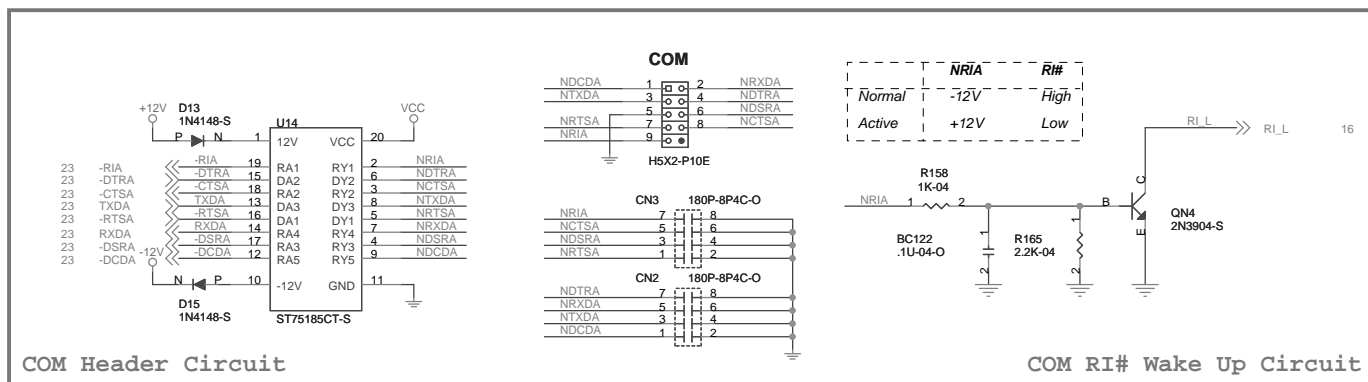
| Title | | |
|-------------------------|-----------------------------|----------------|
| Slot - PCI-EX16/PCI-EX1 | | |
| Size | Document Number | Rev |
| Custom | H61H2-A | 1.0 |
| Date: | Wednesday, January 26, 2011 | Sheet 20 of 31 |



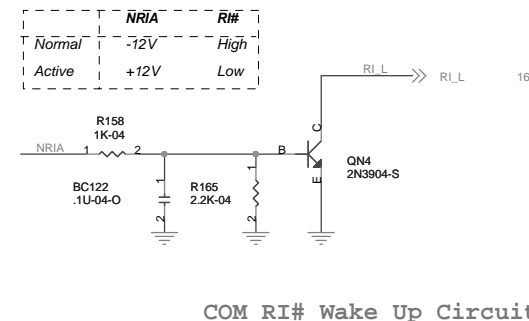
DVI



PS2 Circuit



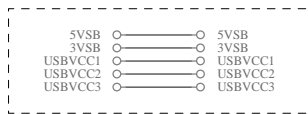
COM Header Circuit



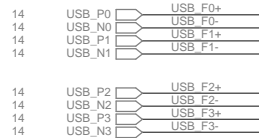
COM RI# Wake Up Circuit

ECS Elitegroup Computer Systems

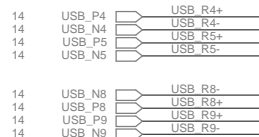
| Title | | | |
|-----------------------|-----------------------------|-------|----------|
| DVI&HDMI CONN&COM&PS2 | | | |
| Size | Document Number | Rev | |
| Custom | H61H2-A | 1.0 | |
| Date: | Wednesday, January 26, 2011 | Sheet | 21 of 31 |



USB FRONT SIDE



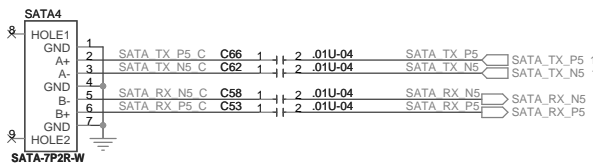
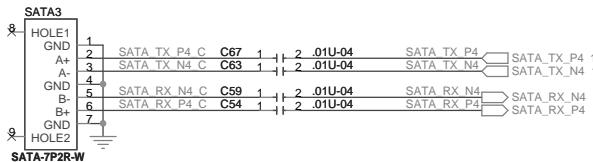
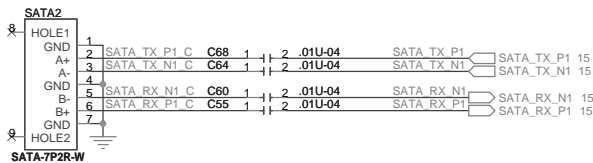
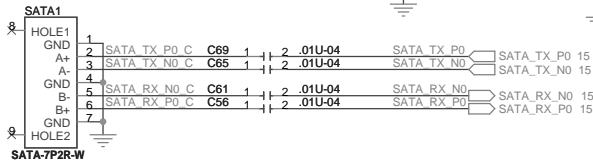
REAR SIDE



4,11,16,23 SLP3_L SLP3_N



Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%



V_1P5_SM

MC3 1U-16VX-06

DIMM_5VDUAL

R75 7.5K-04-O

R74 3.3K-04-O

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

UP7536AMA8S

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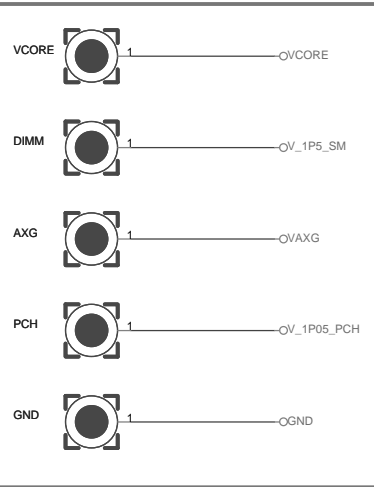
UP7536AMA8S

UP7536AMA8S

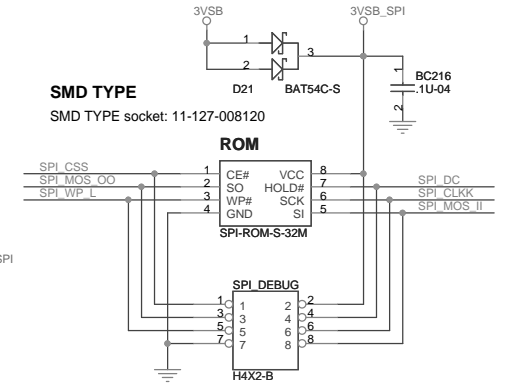
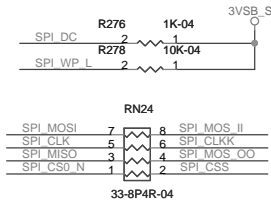
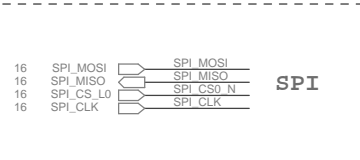
UP7536AMA8S

UP7536AMA8S

UP7536AMA8S



ELI Measure Point

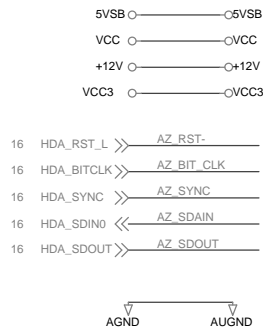


若上SMD SPI ROM, MP or A5後不上ROM Socket.

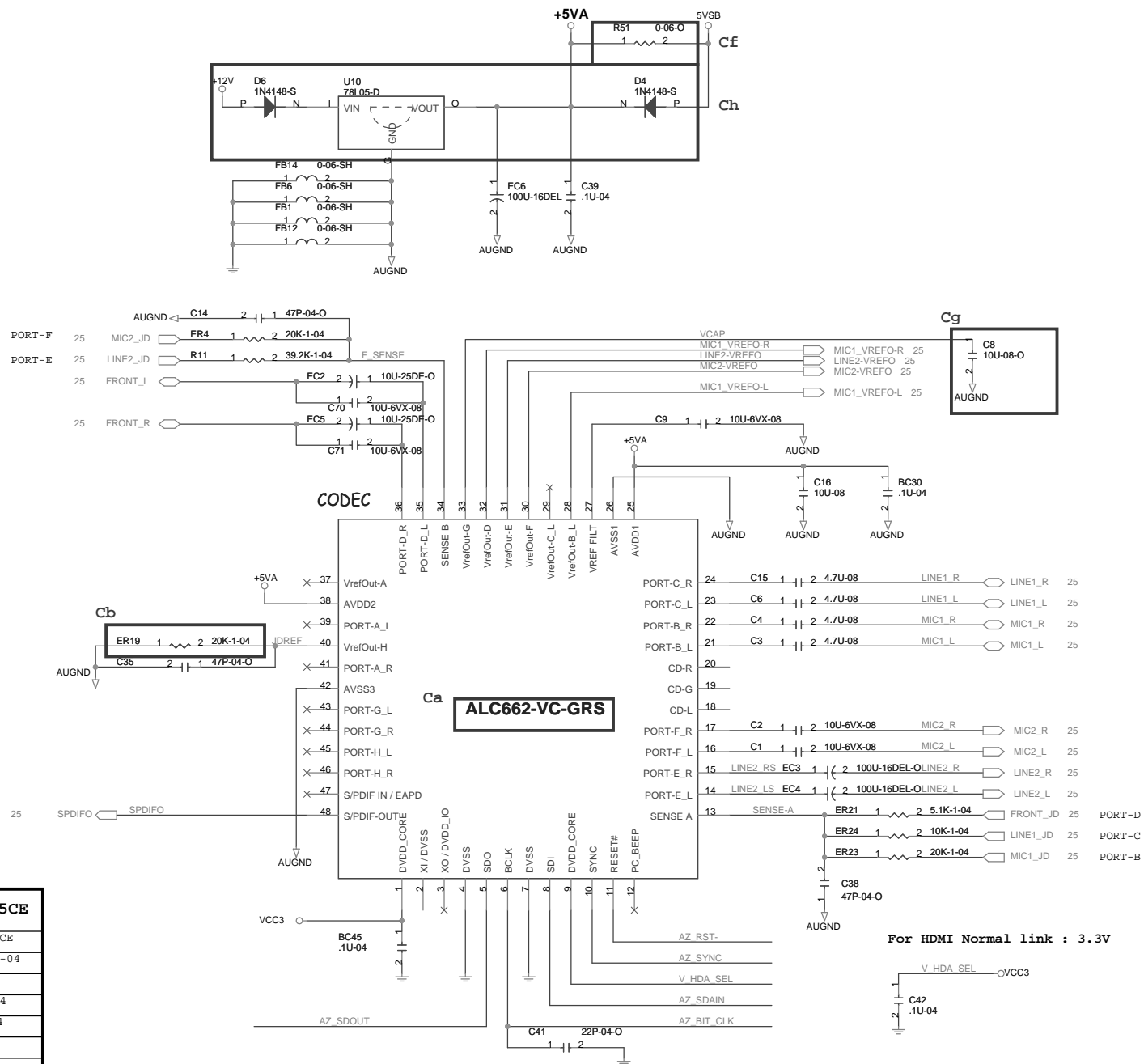
Elitegroup Computer Systems

| Title | | |
|--------------|----------------------------|----------------|
| USB/SATA/SPI | | |
| Size | Document Number | Rev |
| Custom | H61H2-A | 1.0 |
| Date: | Thursday, January 27, 2011 | Sheet 22 of 31 |

External Connection



* VCC1.5 can remove for non-Intel G4X platform



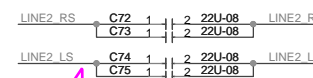
BOM Difference

| Location | ALC662 | VT1705 | VT1705CE |
|----------|---------------|-----------|-----------|
| Ca | ALC662-VC-GRS | VT1705 | VT1705CE |
| Cb | 20K-1-04 | 5.1K-1-04 | 5.1K-1-04 |
| Cc | V | X | X |
| Cd | 2.2K-04 | 3.3K-04 | 3.3K-04 |
| Ce | 75-04 | 75-04 | 75-04 |
| Cf | X | X | V |
| Cg | X | X | V |
| Ch | V | V | X |

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

For HDMI Normal link : 3.3V

For All-Solid Capacitor



ECS Elitegroup Computer Systems

Title: **AUDIO VT1705/ALC662 (CHIP)**

Size: Document Number **H61H2-A** Rev **1.0**

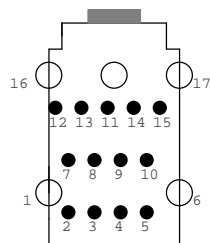
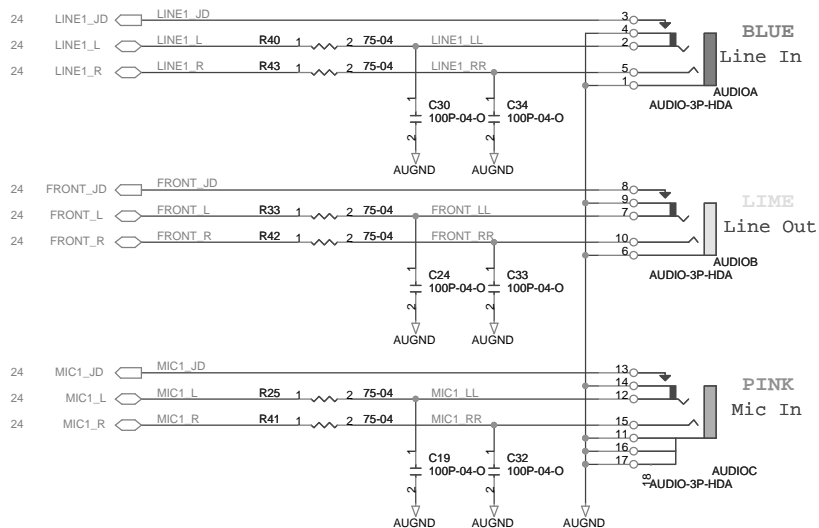
Date: Wednesday, January 26, 2011 Sheet 24 of 31

External Connection

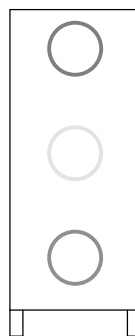
16 FP_AUD_DETECT <-- FP_AUD_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

REAR-AUDIO Non re-tasking for rear panel

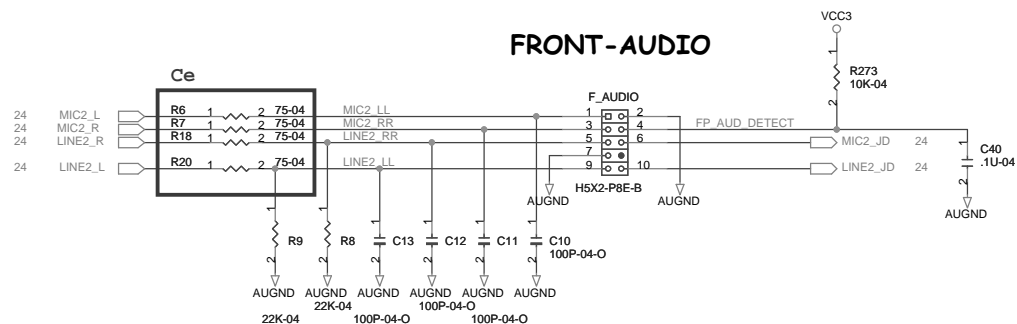


TOP VIEW

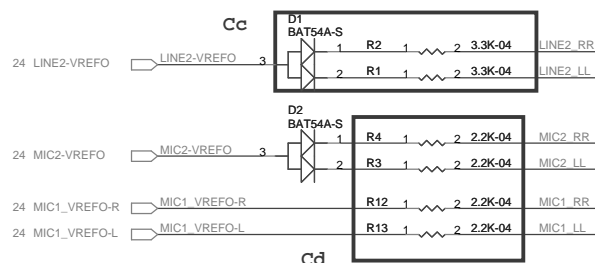


FRONT VIEW

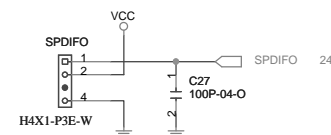
FRONT-AUDIO



MIC Bias



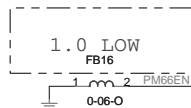
SPDIF-OUT



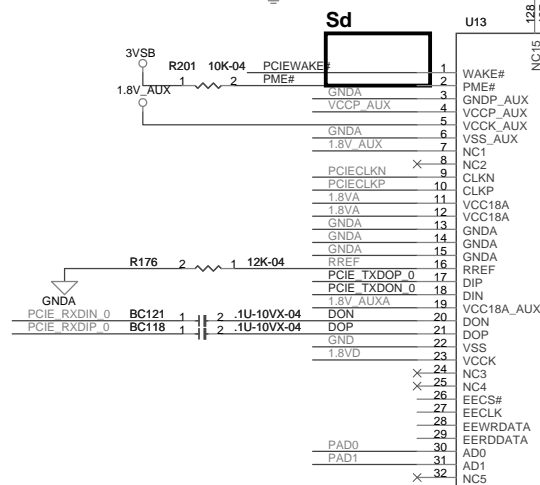
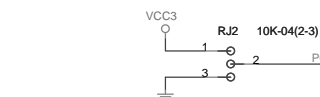
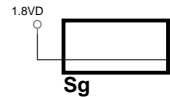
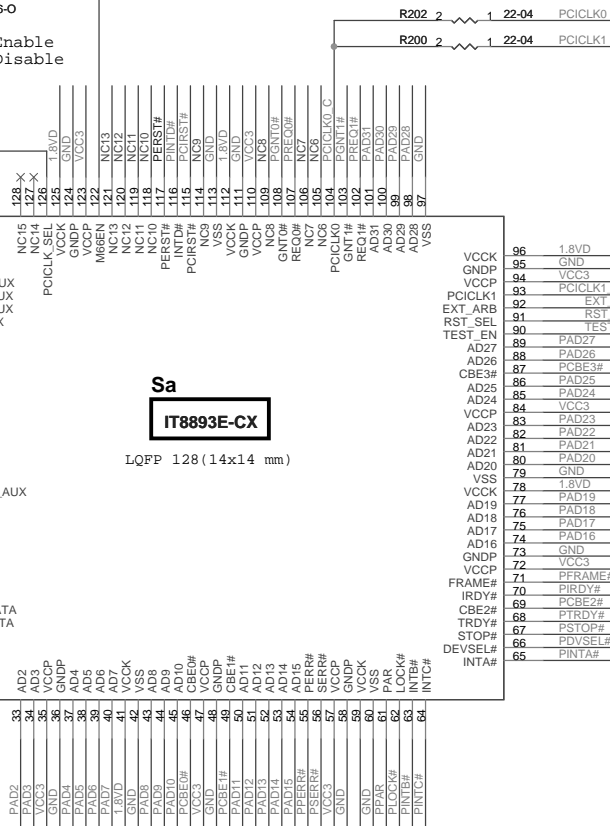
External Connection

The diagram illustrates the external connections for the V100 module. The connections are as follows:

- V_IP8_SFR** is connected to **OV_IP8_SFR**.
- 3VSB** is connected to **OV3VSB**.
- 16,20,28 PCIE_WAKE_L** is connected to **PCIEWAKE#**.
- 14 PCI_TX_P_0** is connected to **PCIE_TXDOP_0**.
- 14 PCI_TX_N_0** is connected to **PCIE_TXDON_0**.
- 15 CK_PE_100M_PCI_H** is connected to **PCIECLKP**.
- 15 CK_PE_100M_PCI_L** is connected to **PCIECLKN**.
- 14 PCI_RX_P_0** is connected to **PCIE_RXDIP_0**.
- 14 PCI_RX_N_0** is connected to **PCIE_RXDIN_0**.
- 4,23,28 SIO_PCIEST2_L** is connected to **PERST#**.

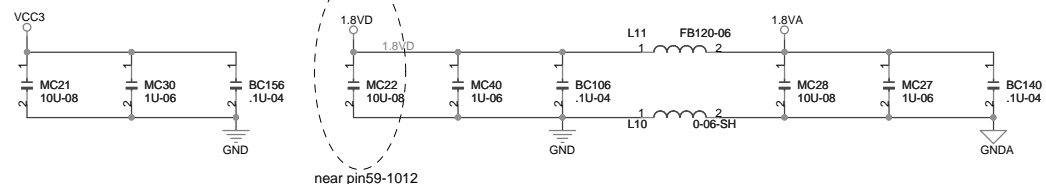


```
1-2: Enable
2-3: Disable
```

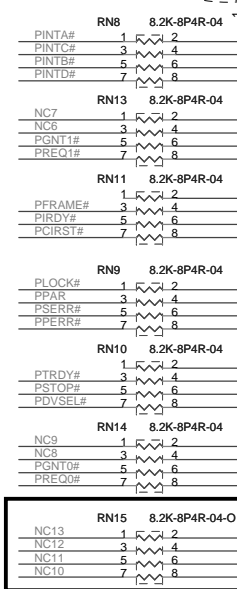
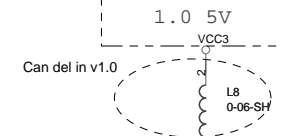
[illegible]

3VSB
1
2
BC153
.1U-04
GND

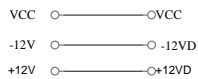
near pin5-1012



| | | |
|---------------|-----------|------------|
| | IT8893AX | IT8893CX |
| Sa | IT8893AX | IT8893E-CX |
| Sb | V | X |
| Sc | V | X |
| Sd | X | V |
| Se page 27 | 0-04(1-2) | 0-04(2-3) |
| Sf | X | V |
| Sa | V | X |

**Sb**

External Connection



COMMON

| | | | |
|----|-----------|---------|---------|
| 26 | PAD[31:0] | PCIRST# | PCIRST# |
| 26 | PCIRST# | PCBE0# | PCBE0# |
| 26 | PCBE0# | PCBE1# | PCBE1# |
| 26 | PCBE1# | PCBE2# | PCBE2# |
| 26 | PCBE2# | PCBE3# | PCBE3# |
| 26 | PME# | PME# | PME# |
| 26 | PM66EN | PM66EN | PM66EN |
| 26 | PFRAME# | PFRAME# | PFRAME# |
| 26 | PIRDY# | PIRDY# | PIRDY# |
| 26 | PSTOP# | PSTOP# | PSTOP# |
| 26 | PDVSEL# | PDVSEL# | PDVSEL# |
| 26 | PPAR | PPAR | PPAR |
| 26 | PSERR# | PSERR# | PSERR# |
| 26 | PPERR# | PPERR# | PPERR# |
| 26 | PCICLK0 | PCICLK0 | PCICLK0 |
| 26 | PLOCK# | PLOCK# | PLOCK# |
| 26 | PINTA# | PINTA# | PINTA# |
| 26 | PINTB# | PINTB# | PINTB# |
| 26 | PINTC# | PINTC# | PINTC# |
| 26 | PINTD# | PINTD# | PINTD# |
| 26 | PREQ0# | PREQ0# | PREQ0# |
| 26 | PGNT0# | PGNT0# | PGNT0# |
| 26 | PCICLK1 | PCICLK1 | PCICLK1 |
| 26 | PREQ1# | PREQ1# | PREQ1# |
| 26 | PGNT1# | PGNT1# | PGNT1# |

| | | | |
|----|-----------|-----------|-----------|
| 14 | PCHINTA_L | PCHINTA_L | PCHINTA_L |
| 14 | PCHINTB_L | PCHINTB_L | PCHINTB_L |
| 14 | PCHINTC_L | PCHINTC_L | PCHINTC_L |
| 14 | PCHINTD_L | PCHINTD_L | PCHINTD_L |
| 14 | PCH_PME_L | PCH_PME_L | PCH_PME_L |

PCI CHIP

| | | | | | |
|-----------|-----|---------|-----------|-----|-----------|
| GND | A1 | TRST# | -12V | B1 | -12VD |
| +12VD | A2 | TCK | GND | B2 | GND |
| VCC | A3 | TMS | GND | B3 | GND |
| VCC | A4 | TDI | GND | B4 | VCC |
| VCC | A5 | +5V | VCC | B5 | VCC |
| PCI INTA# | A6 | INTA# | PCI INTB# | B6 | PCI INTB# |
| PCI INTB# | A7 | INTB# | PCI INTD# | B7 | PCI INTD# |
| VCC | A8 | INTD# | PCI INTA# | B8 | PCI INTA# |
| VCC | A9 | RESVD1 | PRSTN1# | B9 | PRSTN1# |
| VCC | A10 | RESVD2 | PRSTN2# | B10 | PRSTN2# |
| GND | A11 | RESVD | PRSTN2# | B11 | PRSTN2# |
| GND | A12 | GND | PRSTN2# | B12 | GND |
| GND | A13 | GND | PRSTN2# | B13 | GND |
| 3VSB | A14 | 3.3Vaux | RESVD3 | B14 | RESVD3 |
| VCC | A15 | RST# | GND | B15 | GND |
| PGNT0# | A16 | +5V | CLK | B16 | CLK |
| PCBE0# | A17 | GNT# | GND | B17 | GND |
| PCBE1# | A18 | GND | PREQ0# | B18 | PREQ0# |
| PCBE2# | A19 | GND | REQ# | B19 | REQ# |
| PCBE3# | A20 | AD30 | AD30 | B20 | AD30 |
| VCC3 | A21 | 3.3V | AD29 | B21 | AD29 |
| PAD28 | A22 | GND | AD28 | B22 | AD28 |
| PAD26 | A23 | GND | AD27 | B23 | AD27 |
| GND | A24 | GND | AD26 | B24 | AD26 |
| PAD24 | A25 | GND | AD25 | B25 | AD25 |
| VCC3 | A26 | IDSEL | C/BE3# | B26 | C/BE3# |
| PAD22 | A27 | 3.3V | AD23 | B27 | AD23 |
| PAD20 | A28 | GND | AD22 | B28 | AD22 |
| GND | A29 | GND | AD21 | B29 | AD21 |
| PAD18 | A30 | GND | AD19 | B30 | AD19 |
| PAD16 | A31 | 3.3V | AD18 | B31 | AD18 |
| VCC3 | A32 | 3.3V | AD17 | B32 | AD17 |
| PFRAME# | A33 | 3.3V | C/BE2# | B33 | C/BE2# |
| GND | A34 | GND | FRAME# | B34 | FRAME# |
| PIRDY# | A35 | GND | PIRDY# | B35 | PIRDY# |
| PTD# | A36 | GND | PTD# | B36 | PTD# |
| GND | A37 | GND | DESEL# | B37 | DESEL# |
| PSTOP# | A38 | GND | STOP# | B38 | STOP# |
| VCC3 | A39 | 3.3V | LOCK# | B39 | LOCK# |
| SMBCLK1 | A40 | 3.3V | PERR# | B40 | PERR# |
| SMBDAT1 | A41 | 3.3V | PERR# | B41 | PERR# |
| GND | A42 | GND | SERR# | B42 | SERR# |
| PPAR | A43 | 3.3V | PAR | B43 | PAR |
| PAD15 | A44 | 3.3V | C/BE1# | B44 | C/BE1# |
| VCC3 | A45 | 3.3V | AD14 | B45 | AD14 |
| PAD13 | A46 | GND | AD13 | B46 | AD13 |
| PAD11 | A47 | GND | AD12 | B47 | AD12 |
| GND | A48 | GND | AD10 | B48 | AD10 |
| PAD9 | A49 | GND | AD9 | B49 | AD9 |

| | | | | | |
|--------|-----|--------|--------|-----|--------|
| PCBE0# | A52 | C/BE0# | AD8 | B52 | PAD8 |
| VCC3 | A53 | 3.3V | AD7 | B53 | PAD7 |
| PAD6 | A54 | 3.3V | AD6 | B54 | VCC3 |
| PAD4 | A55 | AD4 | AD5 | B55 | PAD5 |
| GND | A56 | AD3 | AD3 | B56 | PAD3 |
| PAD2 | A57 | GND | AD2 | B57 | GND |
| PAD0 | A58 | AD0 | AD1 | B58 | PAD1 |
| VCC | A59 | +5V | AD1 | B59 | VCC |
| REQ64# | A60 | REQ64# | ACK64# | B60 | ACK64# |
| VCC | A61 | +5V | VCC | B61 | VCC |
| VCC | A62 | +5V | VCC | B62 | VCC |

PCI-W

PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD

PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA

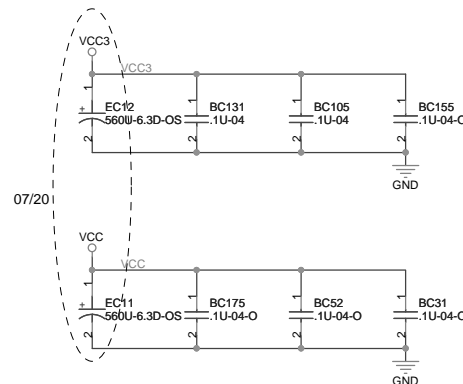
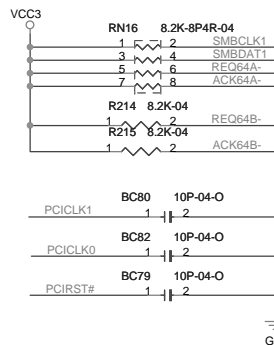
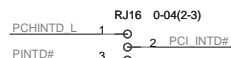
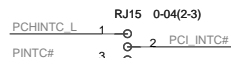
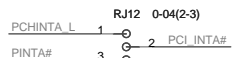
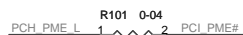
Se For page 26



For ITE chipset auto power-on issue.

As document WW32 2010 Sandy Bridge and Cougar Point Based Platforms Field Message of the Week

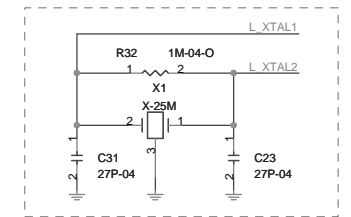
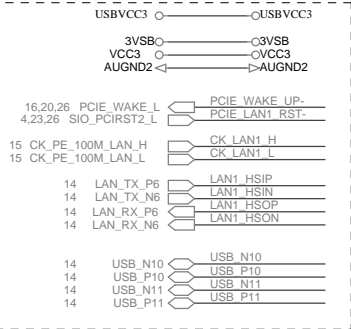
Reserve for Intel PCI Legacy



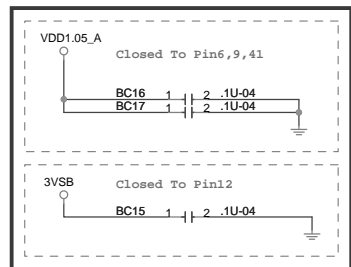
Elitegroup Computer Systems

| | | | |
|--------|-----------------------------|---------|----------|
| Title | Slot - PCI1 & PCI2 | Rev | 1.0 |
| Size | Document Number | H61H2-A | |
| Custom | | | |
| Date: | Wednesday, January 26, 2011 | Sheet | 27 of 31 |

External Connection



Cb



BOM Difference

| | RTL8111E-VL-CG 1000M | RTL8105E-GR 10/100M |
|----|----------------------|---------------------|
| Ca | RTL8111E-VB-GR | RTL8105E-GR |
| Cb | V | X |
| Cc | USBX2-LAN-1000 | USBX2-LAN-100 |
| Cd | X | V |
| Ce | 0-04 | .01U-25VX-04 |
| Cf | V | X |
| Cg | USBX2-LAN-1000 | USBX2-LAN-100 |

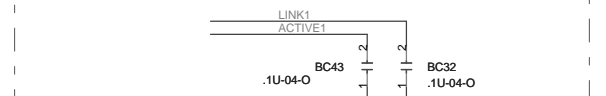
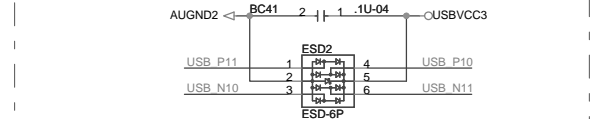
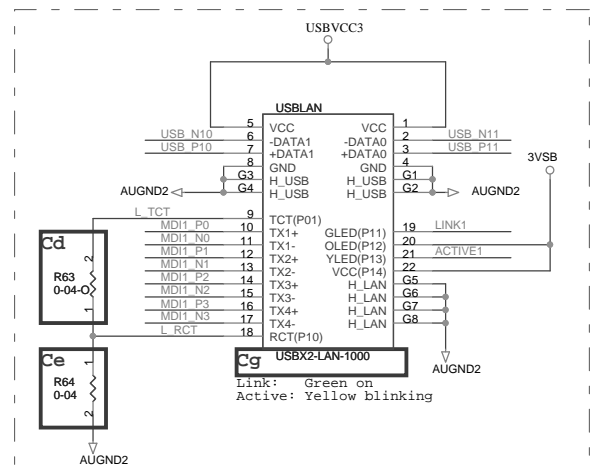
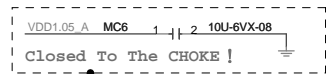
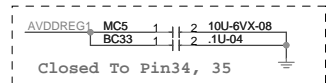
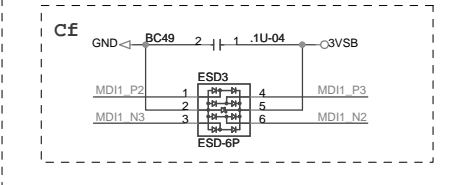
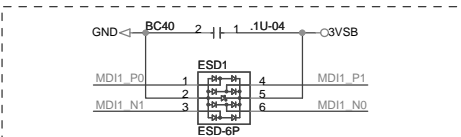
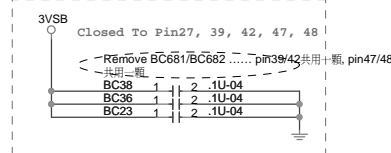
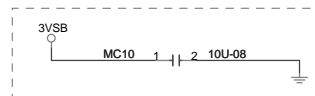
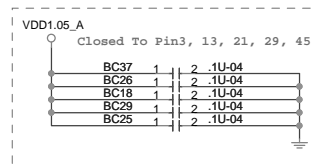
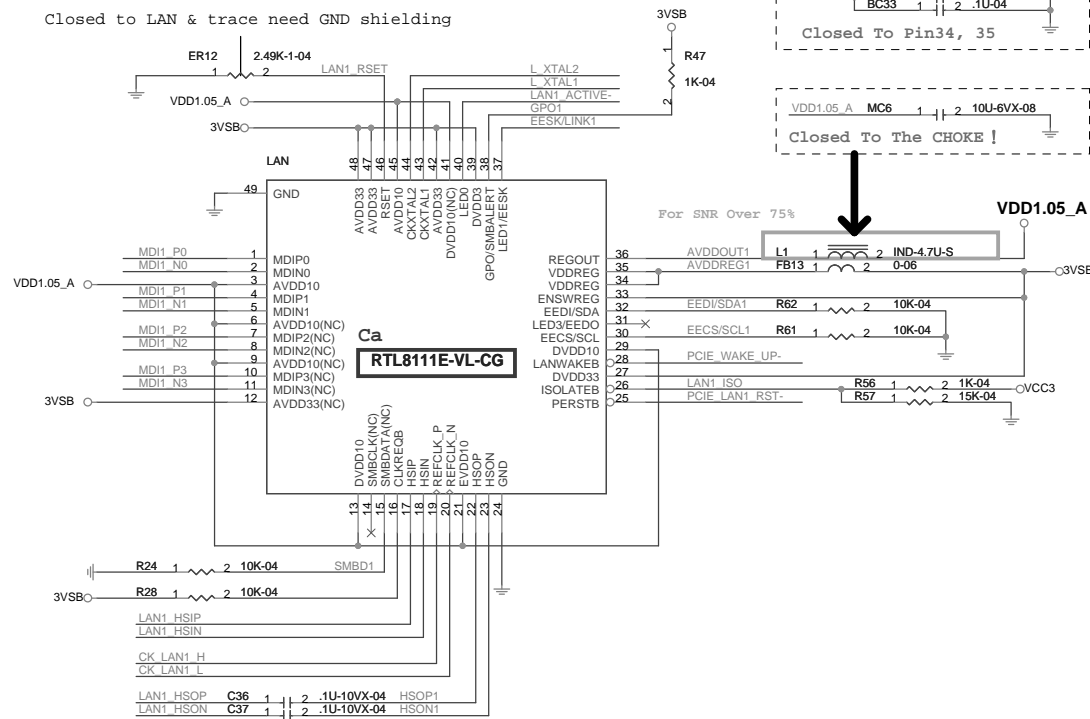
新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端

LAN_HSIP/N請接到SB的PCIE TX端

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

Closed to LAN & trace need GND shielding



| ATX P/S WITH 1A STBY CURRENT | | | | |
|------------------------------|-------|-------|-------|-------|
| 5VSB | 5V | 3.3V | 12V | -12V |
| +/-5% | +/-5% | +/-5% | +/-5% | +/-5% |

| ATX4P |
|-------|
| 12V |
| +/-5% |

| Switching UP1625 4 hases |
|--------------------------------|
|--------------------------------|

Vcore:0.65~1.3V 112Amax

Vauxg:0.65~1.3V 35Amax

| Switching UP1525 1 phase |
|--------------------------------|
|--------------------------------|

V_CPU_VTT:1.05V 17Amax

| Linear OP358 |
|-----------------|
|-----------------|

VCC_SA:0.925V(0.85V) 8.8Amax

| Switching RT8105 |
|---------------------|
|---------------------|

V_DIMM:1.5V 21.5Amax

| DDR3 DIMM (2) 1333MHz | |
|-----------------------|---------|
| VDDQ | 8A_S0 |
| V_SM_VTT | 1.0A_S3 |
| | 0.6A_S0 |

| LDO APL5336 |
|----------------|
|----------------|

DDR_VTT:0.75V

| Linear OP358 |
|-----------------|
|-----------------|

PCH_CORE:1.05V 6.2Amax

Non AMT:
VccASW(ME) short to VIP05_PCH

V_ME:1.05V 1.8Amax

| Linear LM324 |
|-----------------|
|-----------------|

V_SFR:1.8V 1.6Amax

Not support DSW mode:
VccDSW short to 3VSB

| Intel Sandy Bridge CPU | | |
|------------------------|-------------------|----------|
| VCCP | VID 0.25~1.52V | 85A(95W) |
| VAXG | VID 0.25~1.52V | 25A |
| VTT | 1.05V(1V) | 8.5A |
| VCC_SA | 0.925V(0.85V) | 8.8A |
| VCCPLL | 1.8V | 1A |
| VDDQ | 1.5V | 4.5A |

| Intel Cougar Point (TDP 5.5W) | | |
|-------------------------------|-------|---------|
| V_PROC_IO | 1.05V | 1mA |
| VccDMI | 1.05V | 0.057A |
| VccCORE | 1.05V | 1.6A |
| VccIO | 1.05V | 4.07A |
| VccADPLLA | 1.05V | 0.1A |
| VccADPLLB | 1.05V | 0.1A |
| VccCLKDMI | 1.05V | 0.02A |
| VccSSC | 1.05V | 0.105A |
| VccDIFFCLKN | 1.05V | 0.055A |
| VccASW(ME) | 1.05V | 1.61A |
| VccDFTERM | 1.8V | 0.2A |
| VccVRM | 1.8V | 0.159A |
| Vcc3_3 | 3.3V | 0.409A |
| VccADAC | 3.3V | 0.068A |
| VccSPI | 3.3V | 0.02A |
| VccDSW3_3 | 3.3V | 0.003A |
| VccSUS3_3 | 3.3V | 0.097A |
| VccSUSHDA | 3.3V | 0.01A |
| VccRTC | 3.3V | 6uA(G3) |
| V5REF | 5V | 1mA |
| V5REF_SUS | 5V | 1mA |

Battery
3V

| LAN RTL8111E | | |
|-----------------------------|------|-----|
| VDD3P3 | 3.3V | TBD |
| VDD1P05 | 1V | TBD |
| CTRL1P0 internal LVR Output | | |

| SUPER I/O IT8728 | | |
|------------------|------|-----|
| 3VSB | 3.3V | TBD |
| VCC3 | 3.3V | TBD |
| BAT 3.3V | 3.3V | TBD |

| AUDIO ALC662 | | |
|--------------|------|------|
| DVDD 3.3V | 3.3V | 23mA |
| AVDD | 5V | 38mA |

| Fans |
|-----------|
| 12V_200mA |

| SPI |
|-----------|
| VCC3_30mA |

| CRT |
|-------------|
| VCC_1A fuse |

| Flash/NVM |
|-----------|
| VCC3_0.3A |
| 1.8V_0.1A |

| X16 PCIe Slot per | |
|-------------------|----------|
| 3.3V | 3A(S0) |
| 12V | 5.5A(S0) |
| 3.3Vaux | 0.375A |

Total 1 Slot

| X1 PCIe Slot per | |
|------------------|----------|
| 3.3V | 3A(S0) |
| 12V | 0.5A(S0) |
| 3.3Vaux | 0.375A |

Total 3 Slots

| PCI Slot per | |
|--------------|----------|
| 5V | 5A(S0) |
| 12V | 0.5A(S0) |
| 3.3Vaux | 0.375A |
| 3.3V | 7.6A(S0) |

Total 2 Slot

| 5VDUAL Switch IC UP7536 |
|-------------------------------|
|-------------------------------|

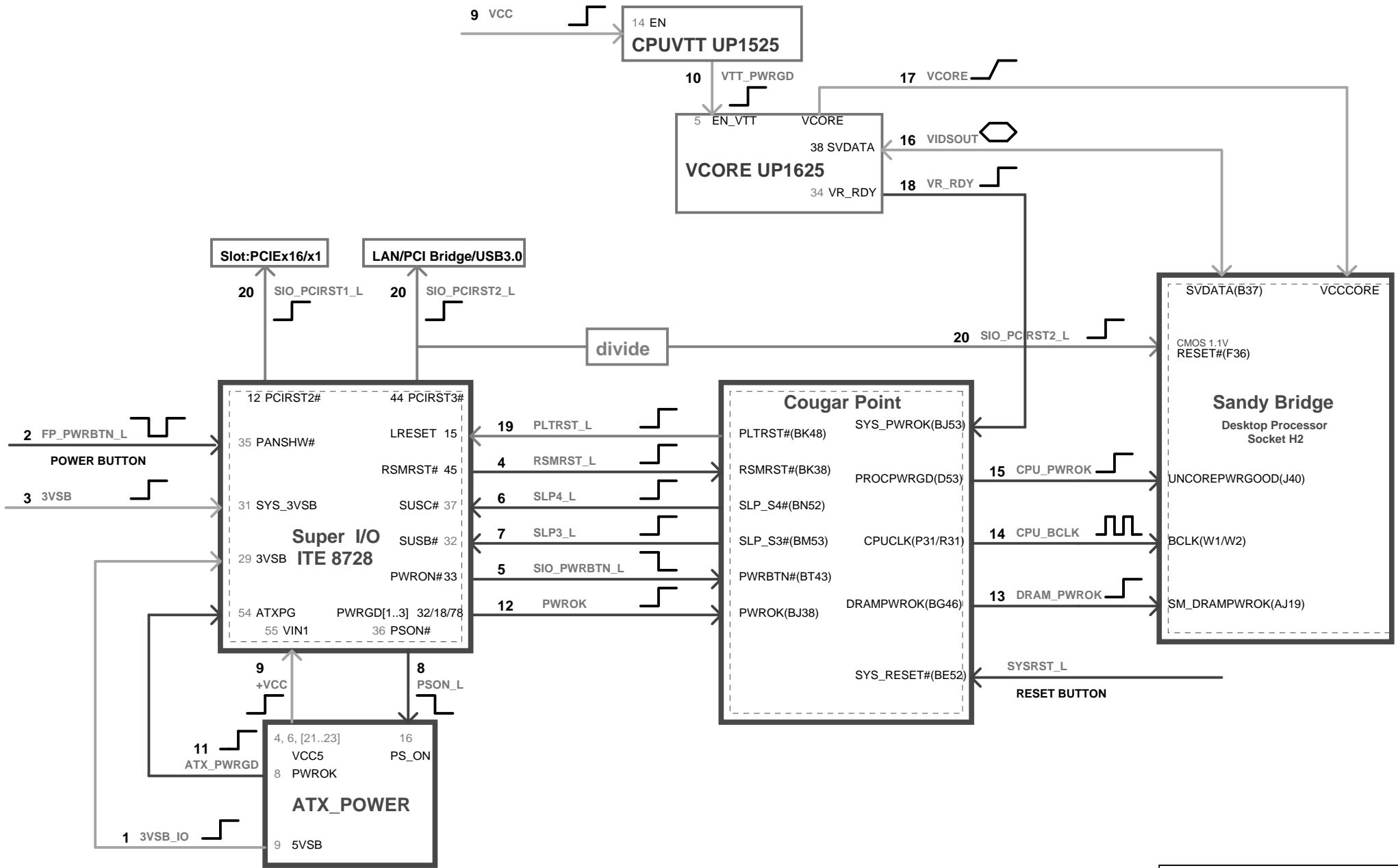
USB_5V

| USB X2 Header | |
|---------------|--------|
| VDD | 5VDual |
| | 2.0A |

| USB X6 IO | |
|-----------|--------|
| VDD | 5VDual |
| | 3.0A |



| | | |
|--------|----------------------------|----------------|
| Title | | Power Delivery |
| Size C | Document Number | H61H2-A |
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| | | Rev 1.0 |



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

